

Model Name: 8I945GMF

Revision 1.0

SHEET

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27	ALC882

SHEET

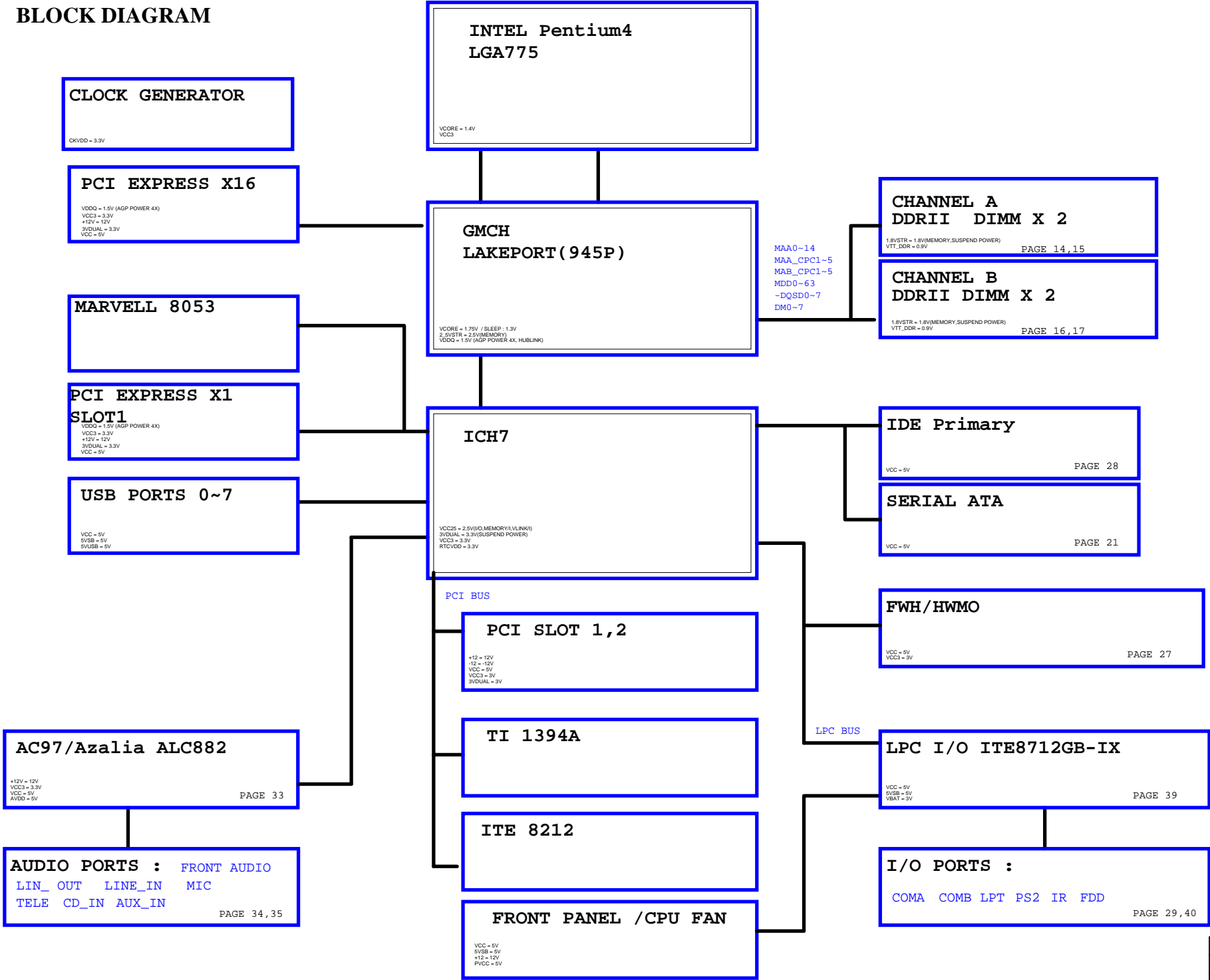
TITLE

28	REAR AUDIO JACK
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30	MARVELL 88E8053
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Gigabyte Technology

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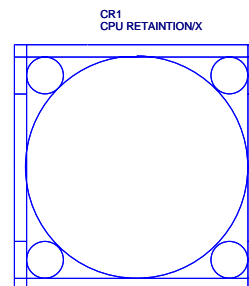
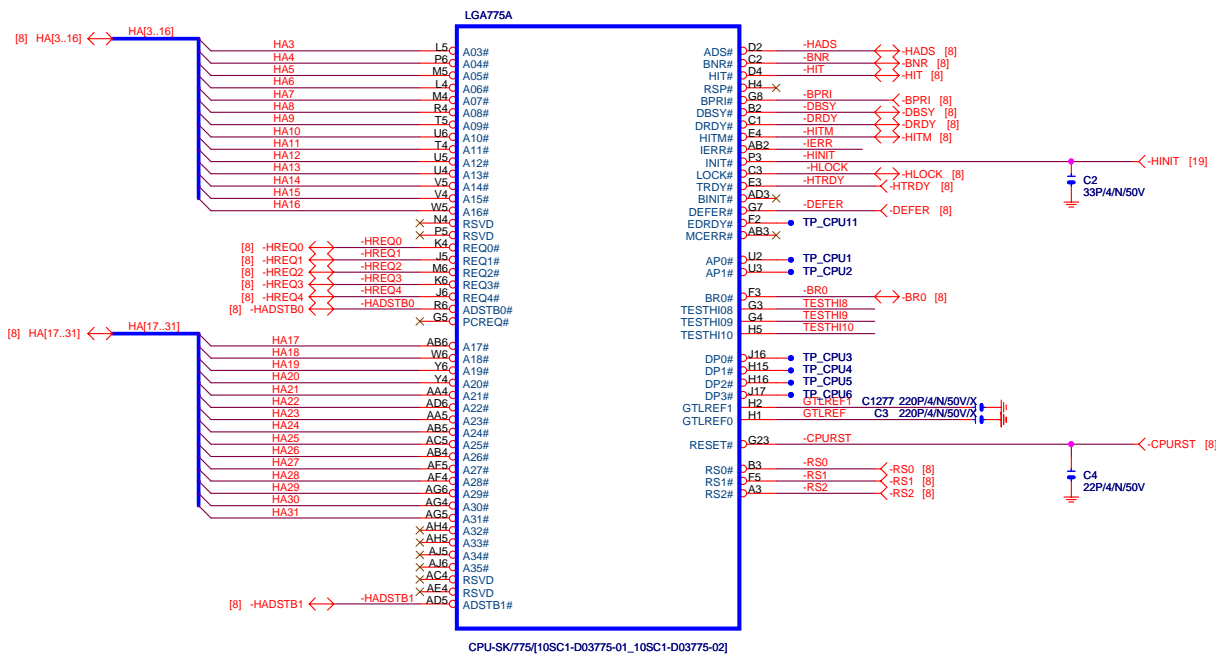
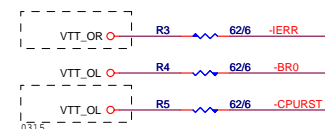
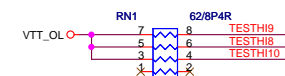
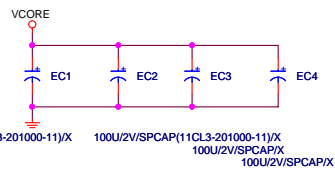
BLOCK DIAGRAM

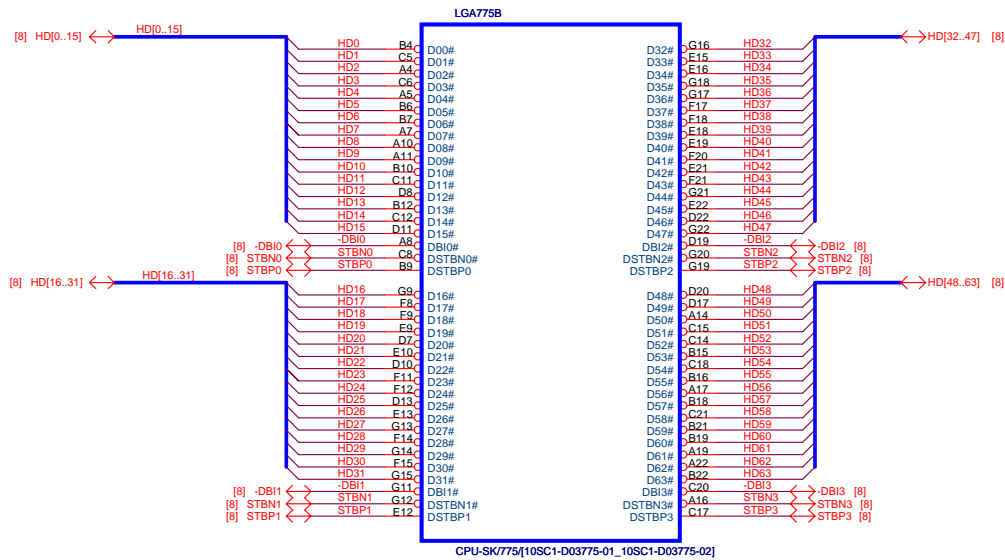


Version: 1.0

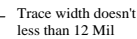
2005/03/25

[illegible][illegible]





VCCA & VCOREPLL
define doesn't same as
old P4 design kit



As close as possible to
CPU socket



限用兩種



FSA	FSB	NA	
FBSSEL0	FBSSEL1	FBSSEL3	Clock
1	0	1	100MHz
1	0	0	133MHz
1	1	0	166MHz
0	1	0	200MHz
0	0	0	266MHz

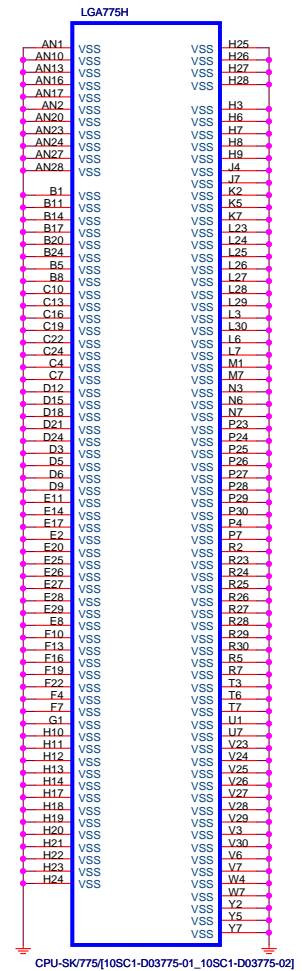
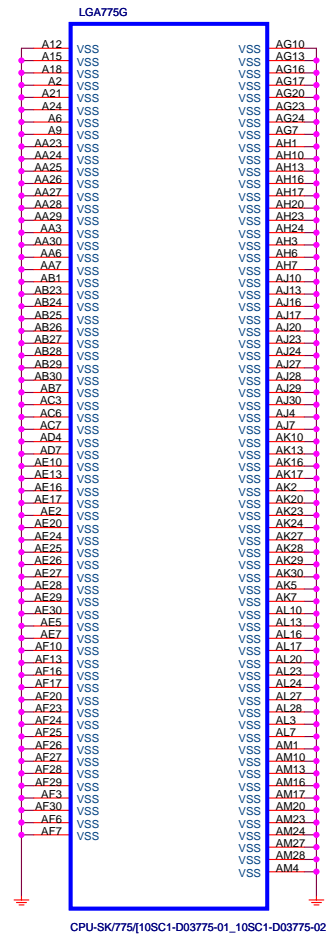
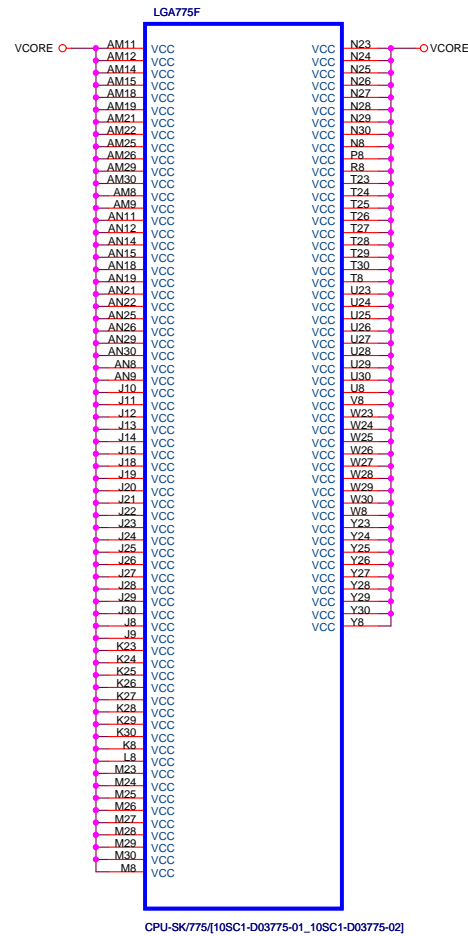
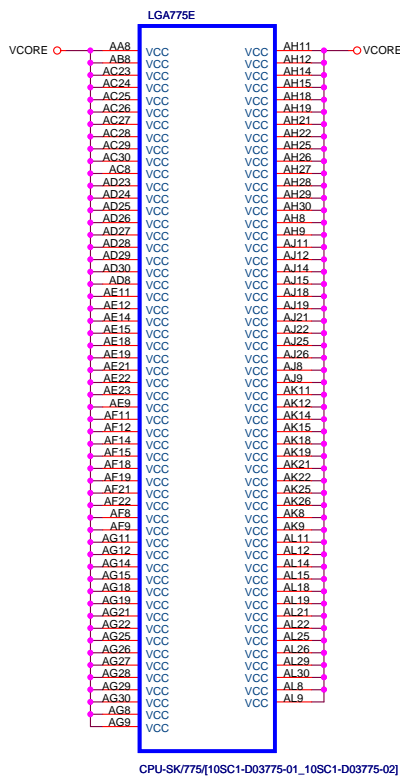


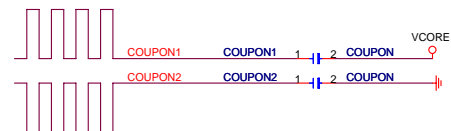
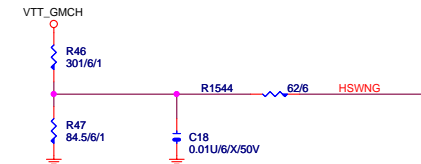
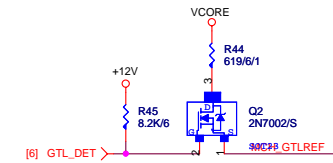
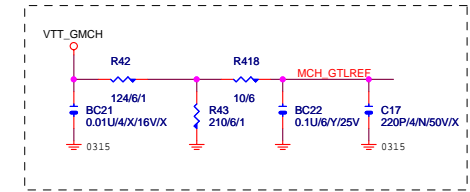
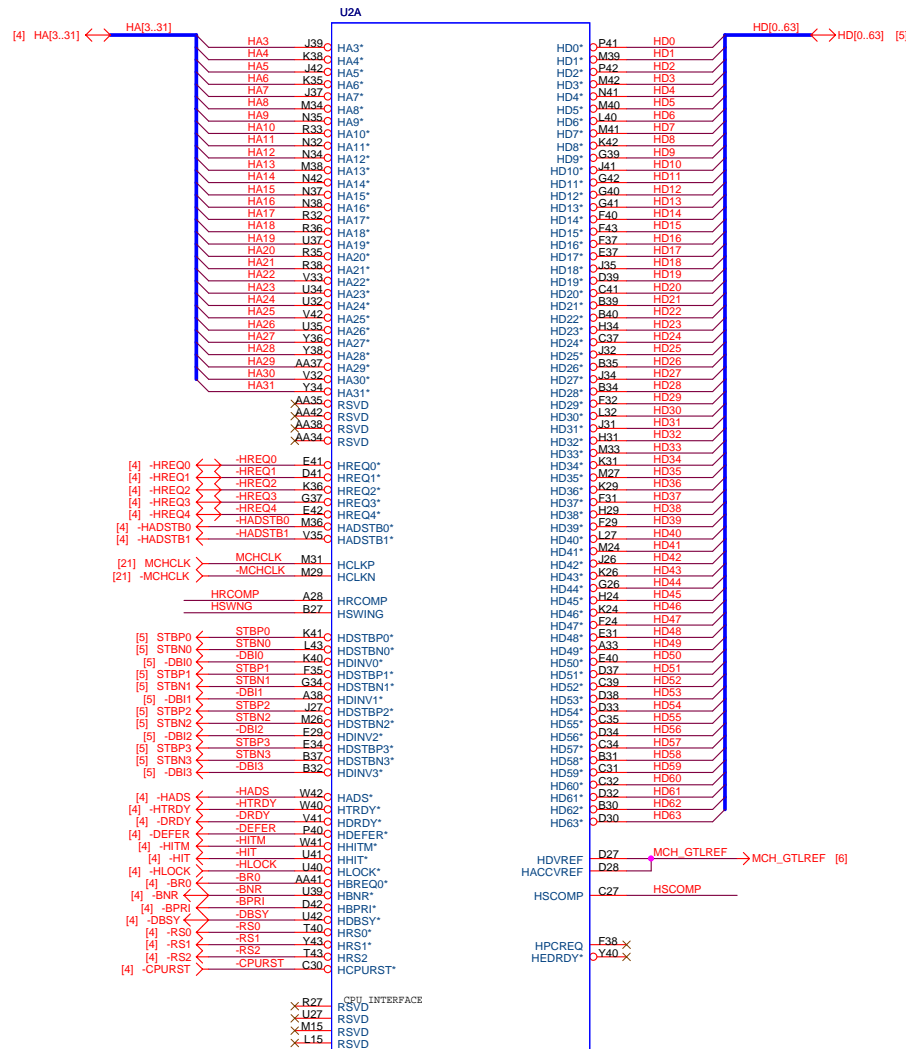
The schematic diagram illustrates the test setup for the 62/8P4R device. The device is shown with pins 1 through 8. The connections are as follows:

- Pin 1:** Connected to R35 (62/6) and TDO.
- Pin 2:** Connected to R36 (62/6) and -TRST.
- Pin 3:** Connected to R37 (62/6) and TCK.
- Pin 4:** Connected to R32 (62/6) and -FORCEPR.
- Pin 5:** Connected to R29 (680/6) and VID3.
- Pin 6:** Connected to R30 (680/6) and VID5.
- Pin 7:** Connected to R29 (680/6) and VID2.
- Pin 8:** Connected to R30 (680/6) and VID0.

The device is also connected to VTT_OR and VTT_PWRGD. Power supplies are connected to the device: 0.1uF/5V/25V to pins 1 and 2, and 0.1uF/6V/25V to pins 3 and 4.

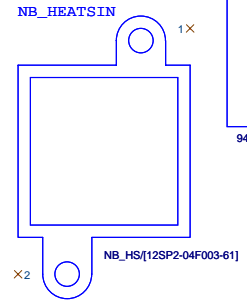
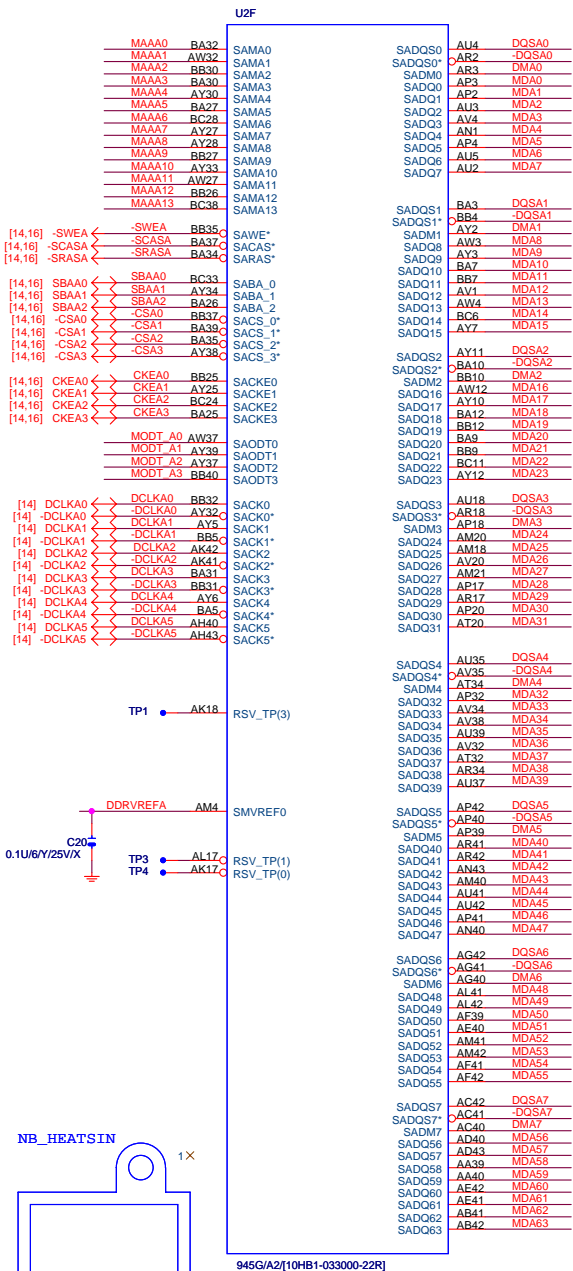
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P4_LGA775-B			
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GMCH-HOST			
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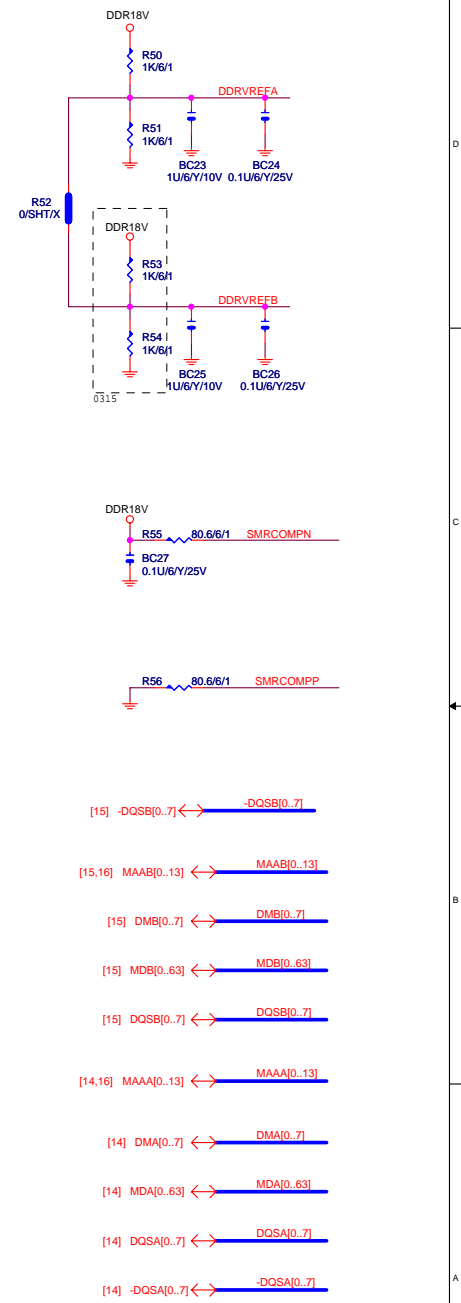
MODT_A[0..3] ↔ MODT_A[0..3] [14,16]

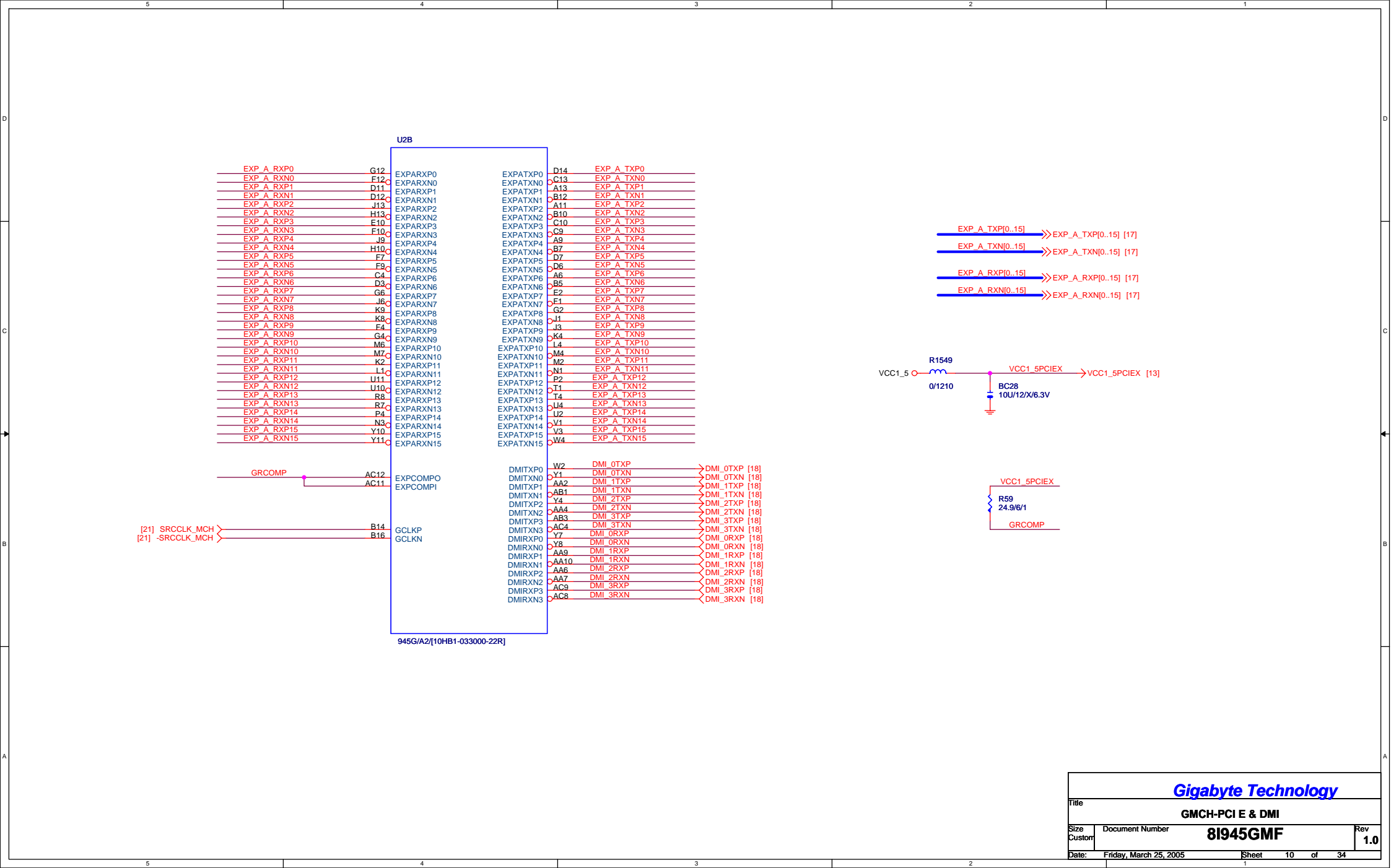


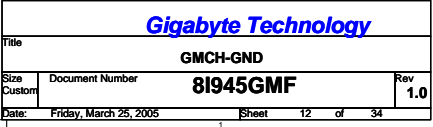
U2G

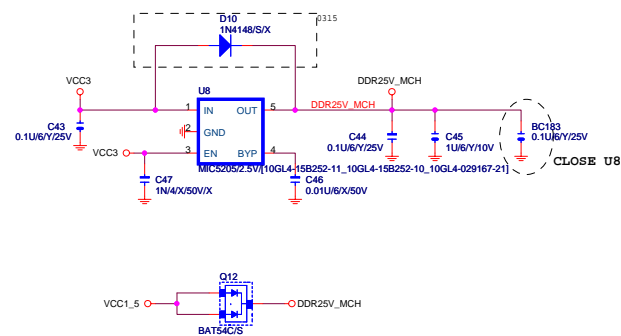
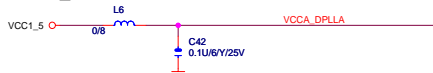
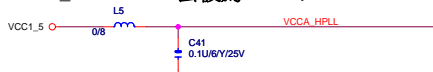
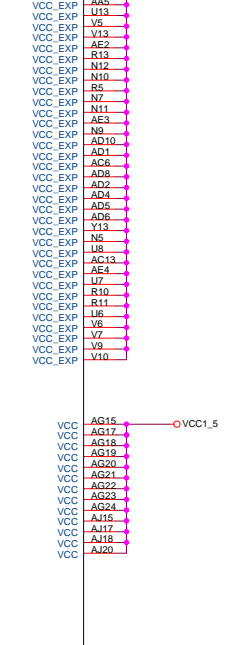
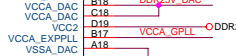
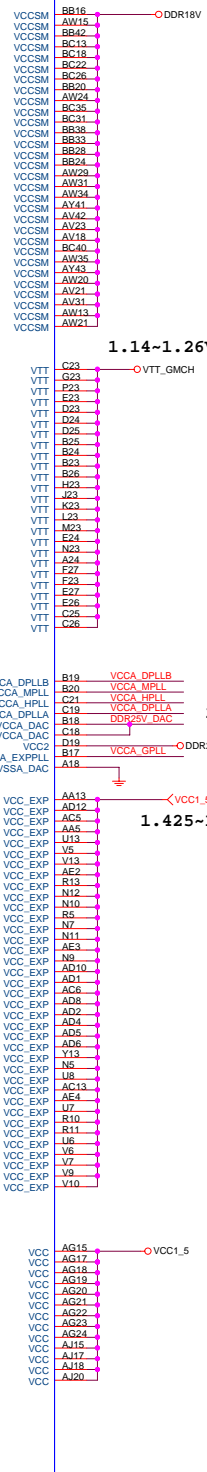
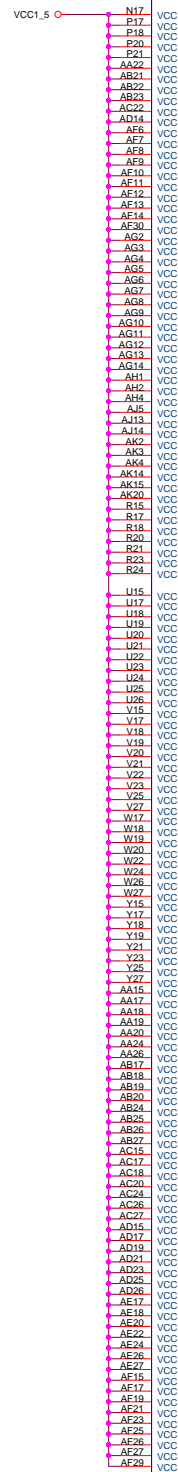


MODT_B[0..3] ↔ MODT_B[0..3] [15,16]

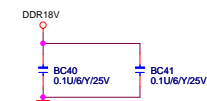
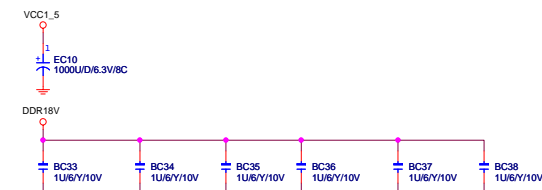
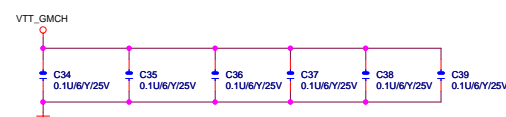


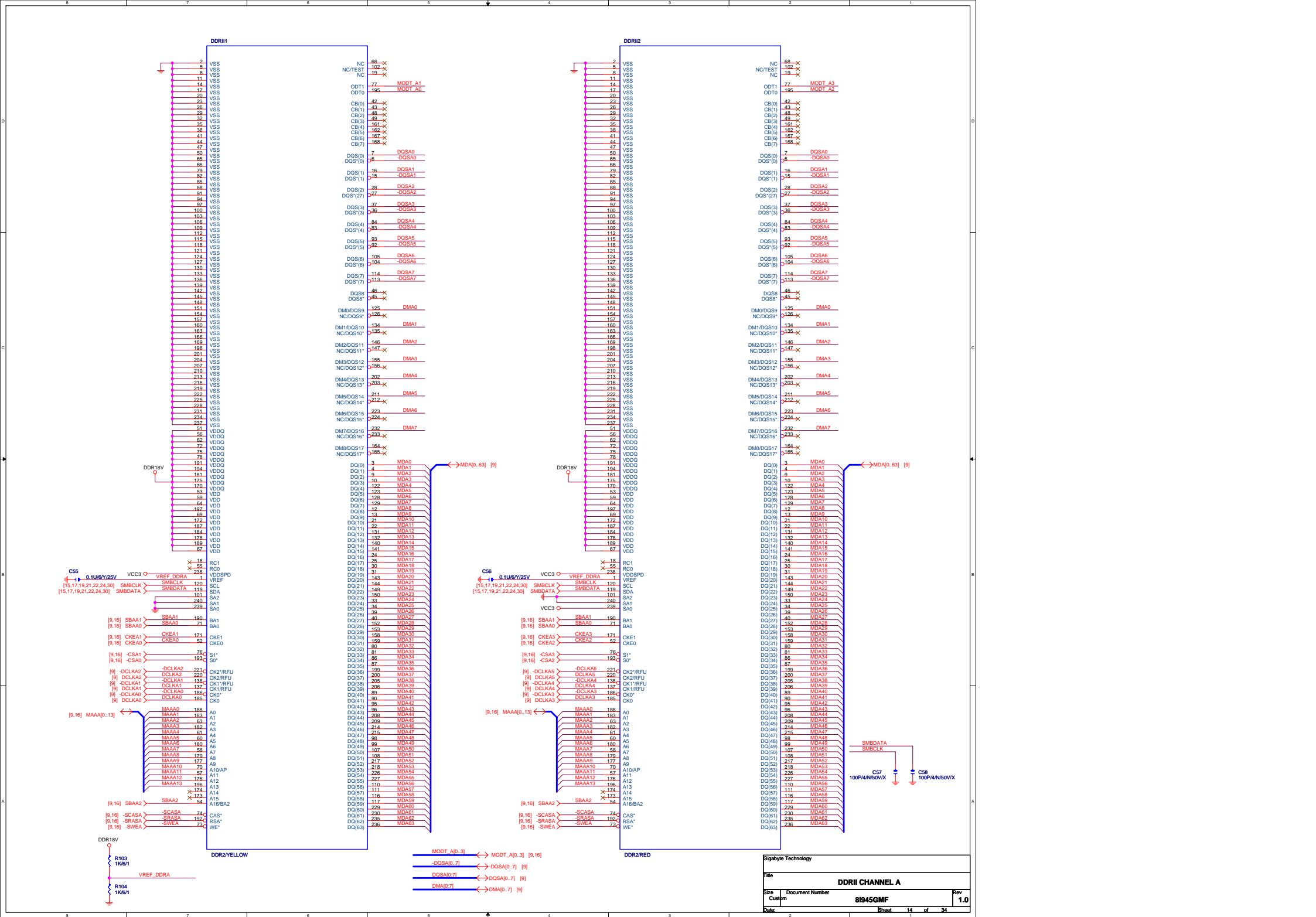


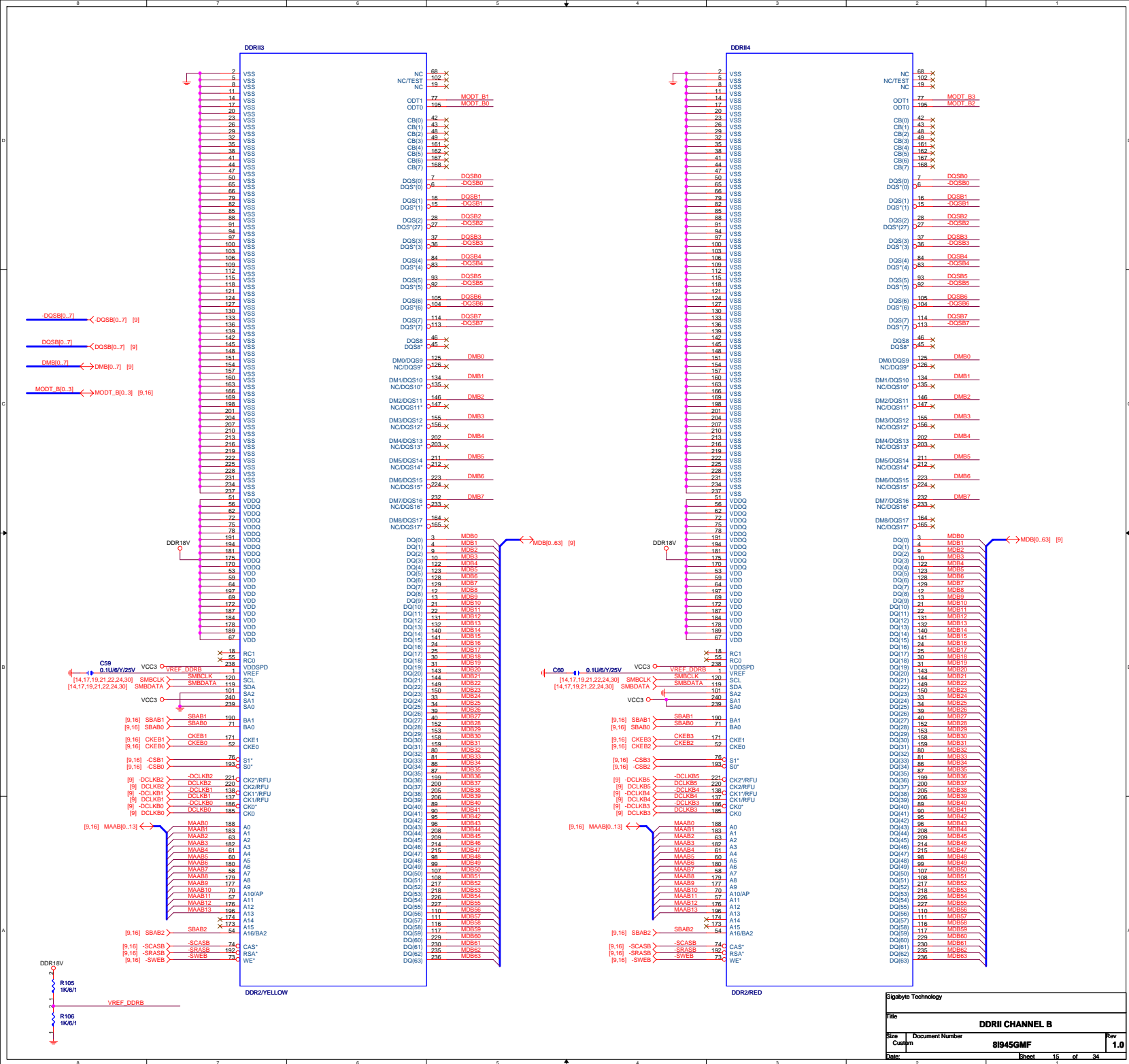




945 Design Guide rev1.5 spec.
VCCA_EXPPLL=VCCA_GPLL=45mA(1.425V~1.575V)
VCCA_HPLL>50mA 公板爲200mA(1.425V~1.575V)
VCCA_DPLLA=65mA(1.425V~1.575V)
VCCA_DPLLB=65mA(1.425V~1.575V)
VCCA_MPLL>50mA(1.425V~1.575V)
VCCA_DAC=DDR25V DAC=70mA(2.375~2.625V)

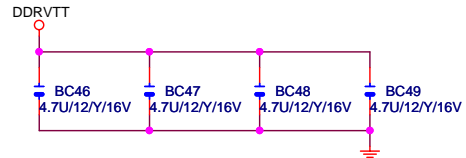
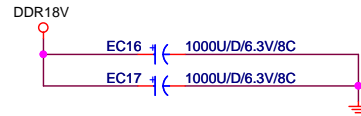
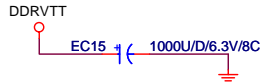




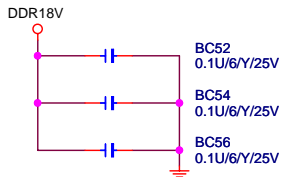


DDR TERMINATION CHANNEL A

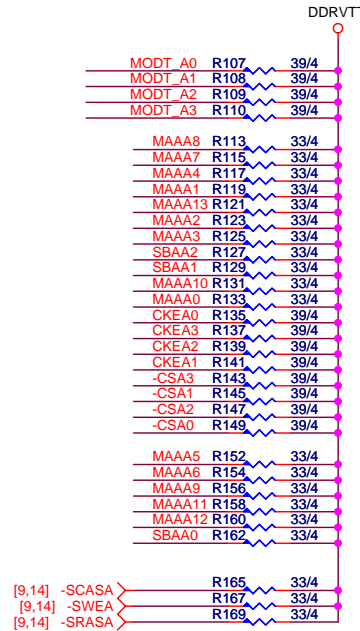
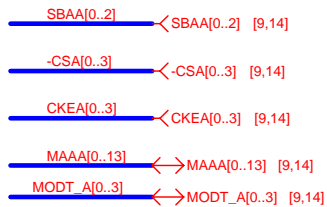
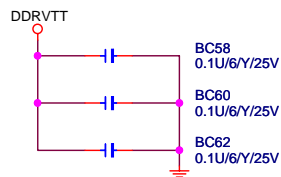
DDRVTT Decouple



DDR18V Decouple

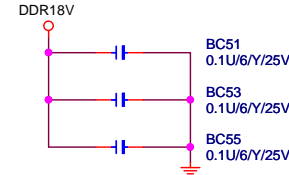


DDRVTT Decouple

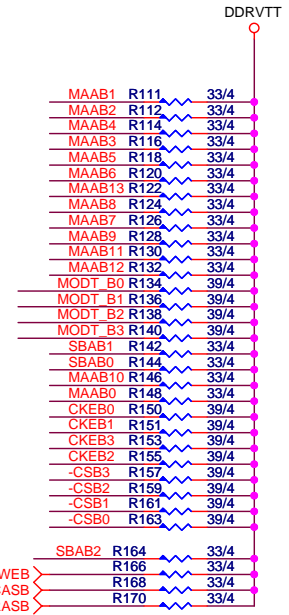
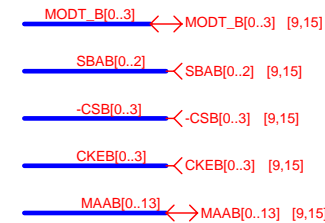
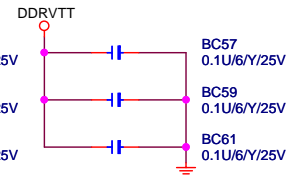


DDR TERMINATION CHANNEL B

DDR18V Decouple

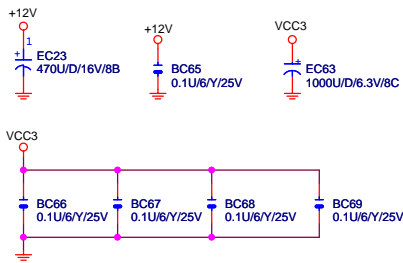


DDRVTT Decouple

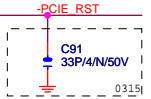
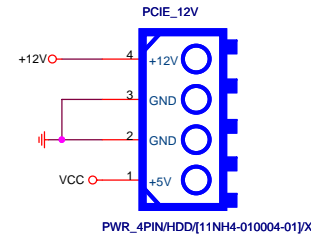
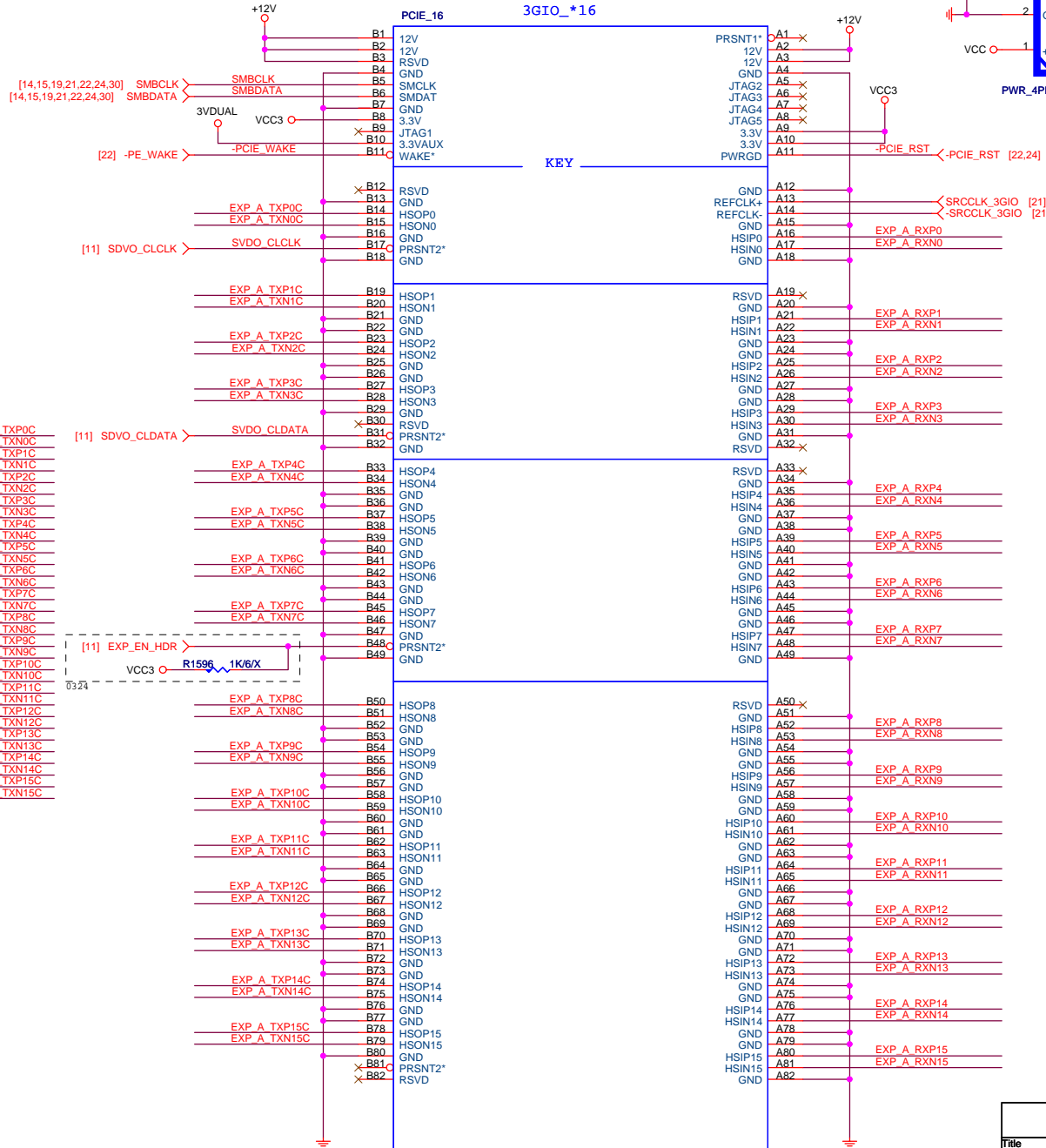


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DDRII TERMINATOR



PCIESLOT-164DN-2



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EXP_A_TXN0[0..15] >>> EXP_A_TXN[0..15] [10]

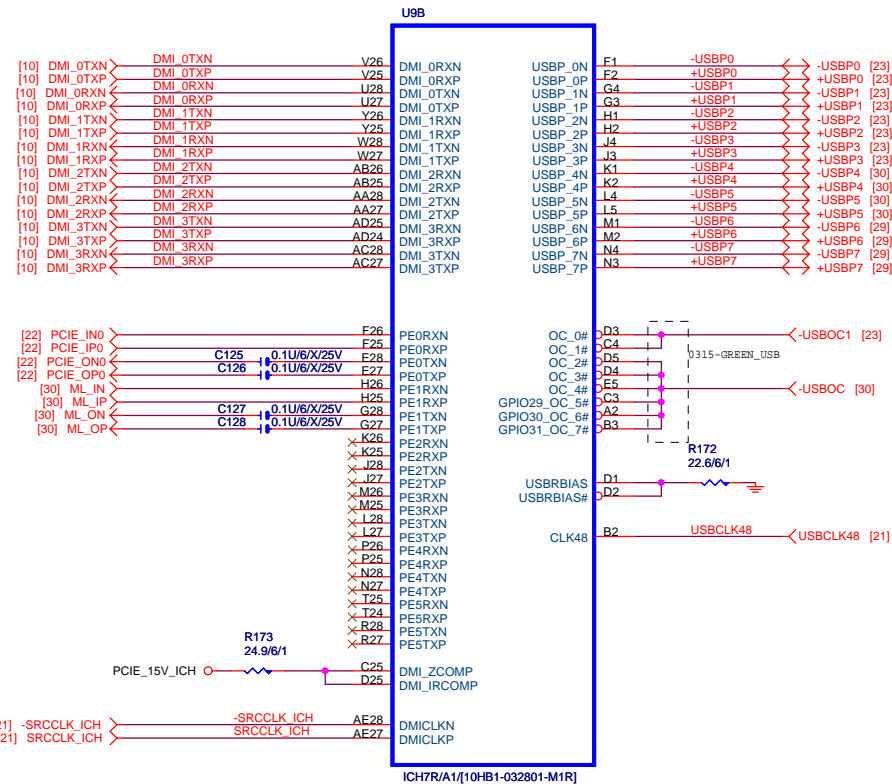
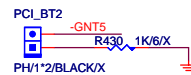
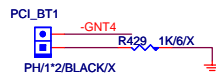
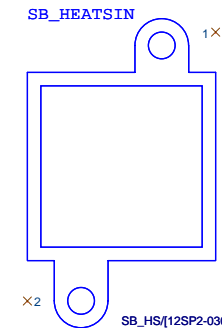
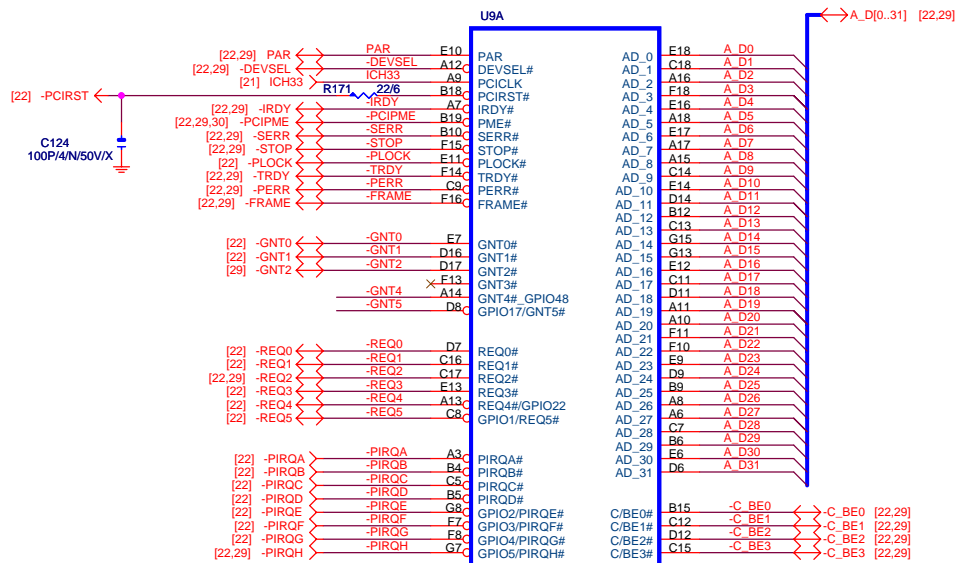
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EXP_A_TXN0	C93	0.1U/6Y/25V	EXP_A_TXN0C
EXP_A_TXP1	C94	0.1U/6Y/25V	EXP_A_TXP1C
EXP_A_TXN1	C95	0.1U/6Y/25V	EXP_A_TXN1C
EXP_A_TXP2	C96	0.1U/6Y/25V	EXP_A_TXP2C
EXP_A_TXN2	C97	0.1U/6Y/25V	EXP_A_TXN2C
EXP_A_TXP3	C98	0.1U/6Y/25V	EXP_A_TXP3C
EXP_A_TXN3	C99	0.1U/6Y/25V	EXP_A_TXN3C
EXP_A_TXP4	C100	0.1U/6Y/25V	EXP_A_TXP4C
EXP_A_TXN4	C101	0.1U/6Y/25V	EXP_A_TXN4C
EXP_A_TXP5	C102	0.1U/6Y/25V	EXP_A_TXP5C
EXP_A_TXN5	C103	0.1U/6Y/25V	EXP_A_TXN5C
EXP_A_TXP6	C104	0.1U/6Y/25V	EXP_A_TXP6C
EXP_A_TXN6	C105	0.1U/6Y/25V	EXP_A_TXN6C
EXP_A_TXP7	C106	0.1U/6Y/25V	EXP_A_TXP7C
EXP_A_TXN7	C107	0.1U/6Y/25V	EXP_A_TXN7C
EXP_A_TXP8	C108	0.1U/6Y/25V	EXP_A_TXP8C
EXP_A_TXN8	C109	0.1U/6Y/25V	EXP_A_TXN8C
EXP_A_TXP9	C110	0.1U/6Y/25V	EXP_A_TXP9C
EXP_A_TXN9	C111	0.1U/6Y/25V	EXP_A_TXN9C
EXP_A_TXP10	C112	0.1U/6Y/25V	EXP_A_TXP10C
EXP_A_TXN10	C113	0.1U/6Y/25V	EXP_A_TXN10C
EXP_A_TXP11	C114	0.1U/6Y/25V	EXP_A_TXP11C
EXP_A_TXN11	C115	0.1U/6Y/25V	EXP_A_TXN11C
EXP_A_TXP12	C116	0.1U/6Y/25V	EXP_A_TXP12C
EXP_A_TXN12	C117	0.1U/6Y/25V	EXP_A_TXN12C
EXP_A_TXP13	C118	0.1U/6Y/25V	EXP_A_TXP13C
EXP_A_TXN13	C119	0.1U/6Y/25V	EXP_A_TXN13C
EXP_A_TXP14	C120	0.1U/6Y/25V	EXP_A_TXP14C
EXP_A_TXN14	C121	0.1U/6Y/25V	EXP_A_TXN14C
EXP_A_TXP15	C122	0.1U/6Y/25V	EXP_A_TXP15C
EXP_A_TXN15	C123	0.1U/6Y/25V	EXP_A_TXN15C

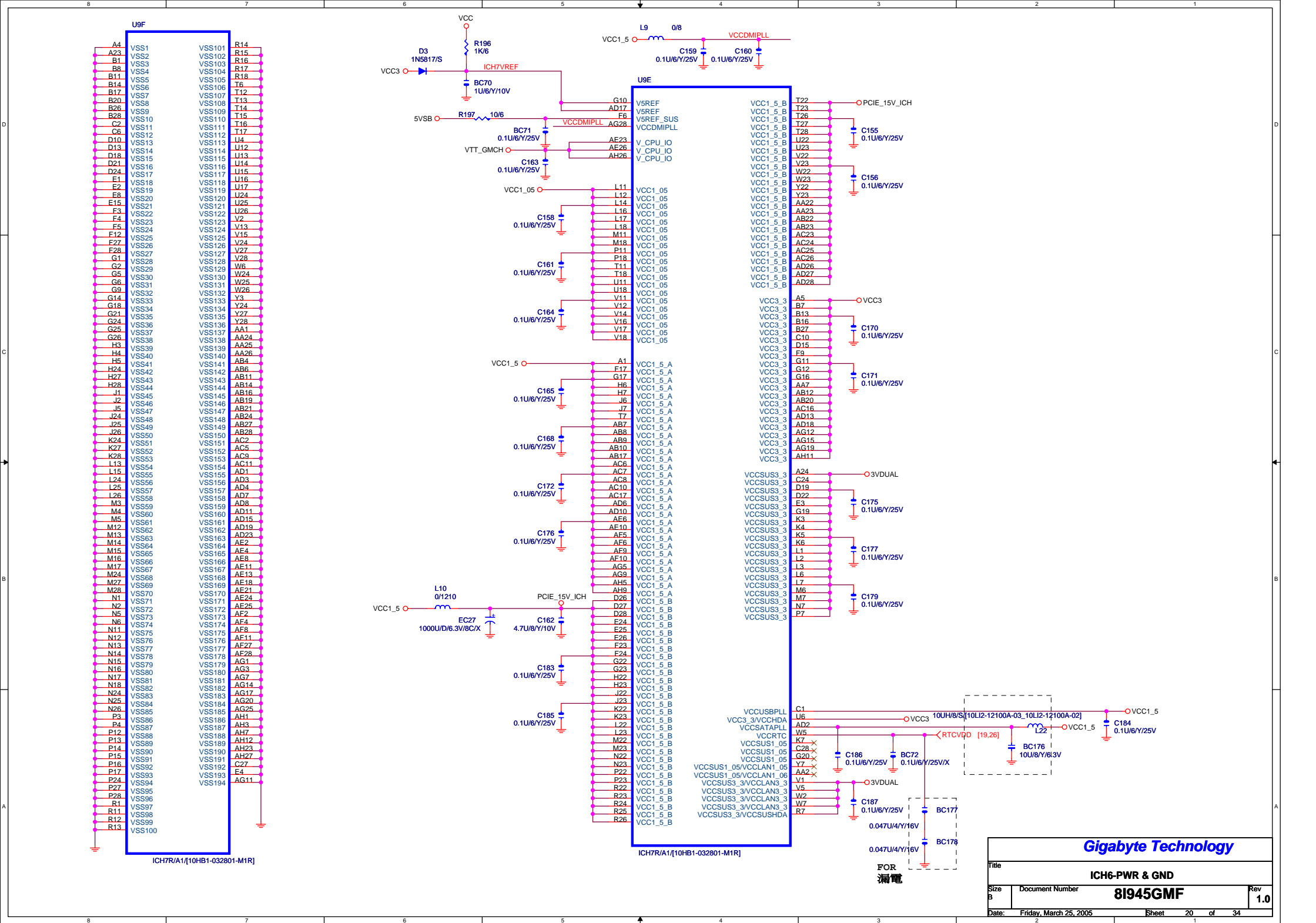
EXP_A_RXP0[0..15] >>> EXP_A_RXP[0..15] [10]
EXP_A_RXN0[0..15] >>> EXP_A_RXN[0..15] [10]

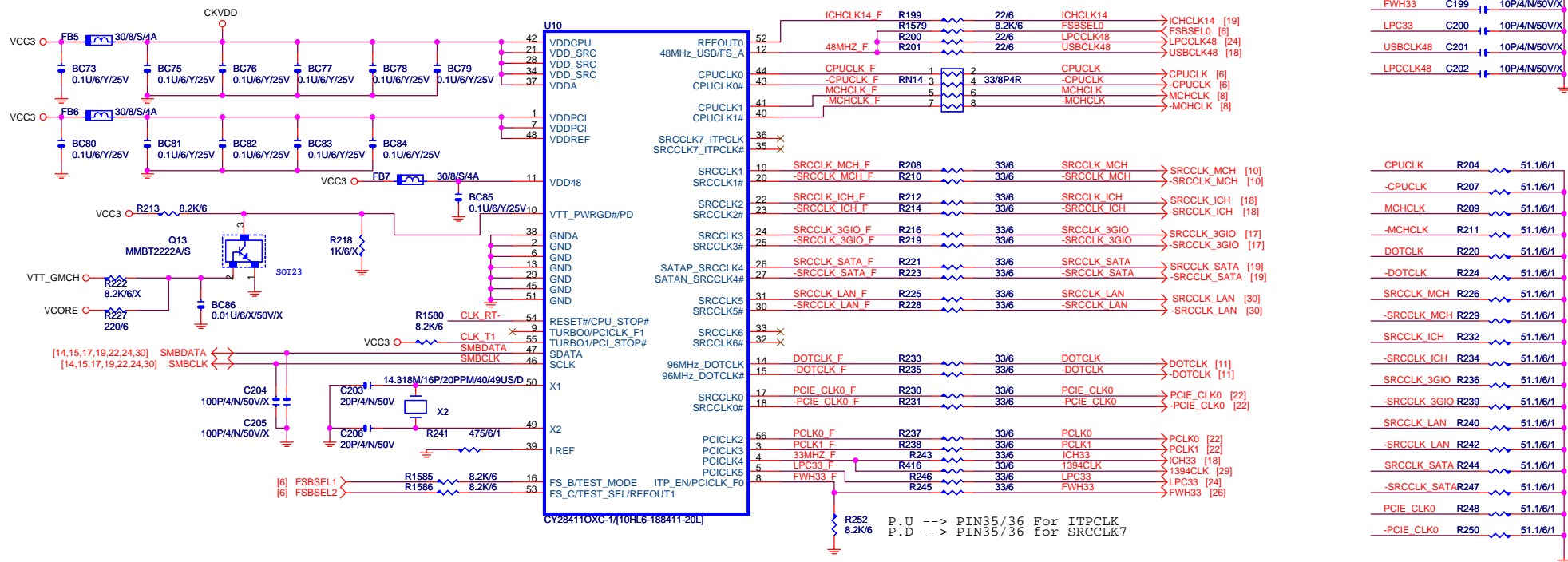
PCI-E16/L[11AC1-021164-21_11AC1-021164-22]

0325

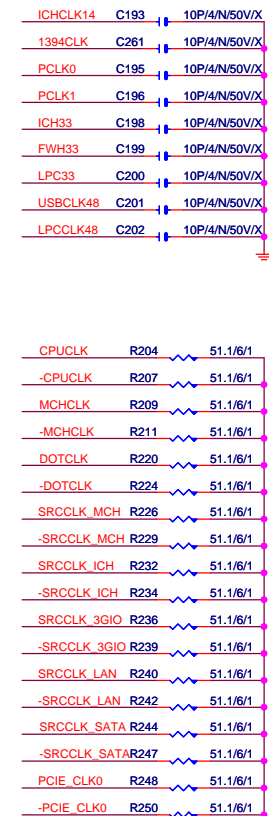
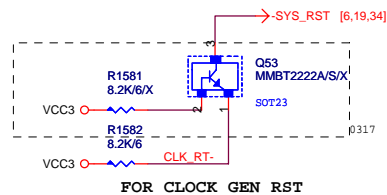
Gigabyte Technology		
Title		
PCI EXPRESS * 16		
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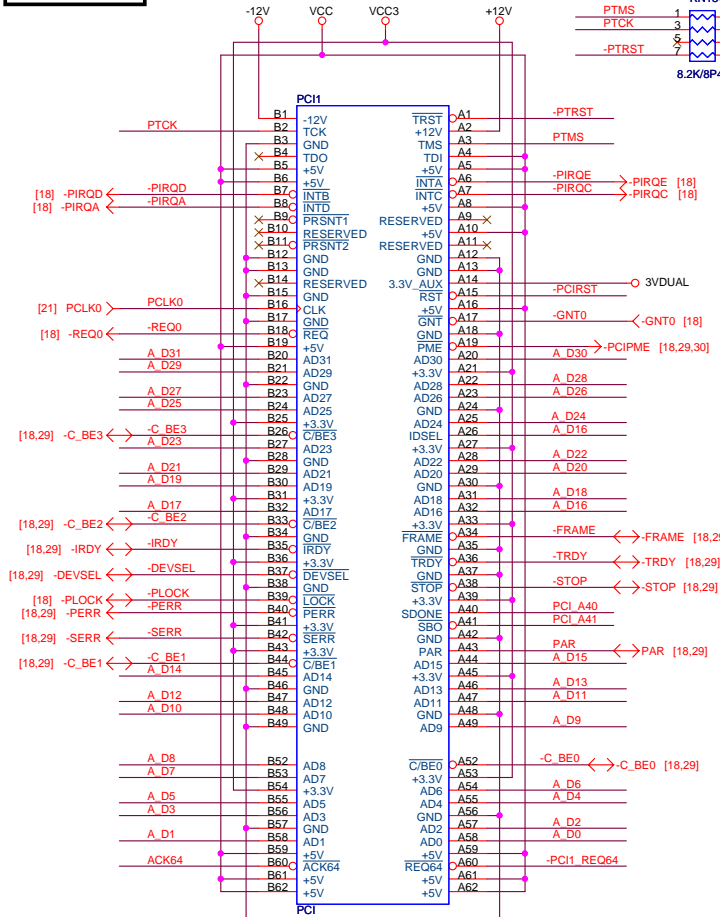
CY284110XC-1無RESET,不可上Q53,否則CPU_STOP#產生,造成CPURST- DELAY 200ms(spec>1ms)



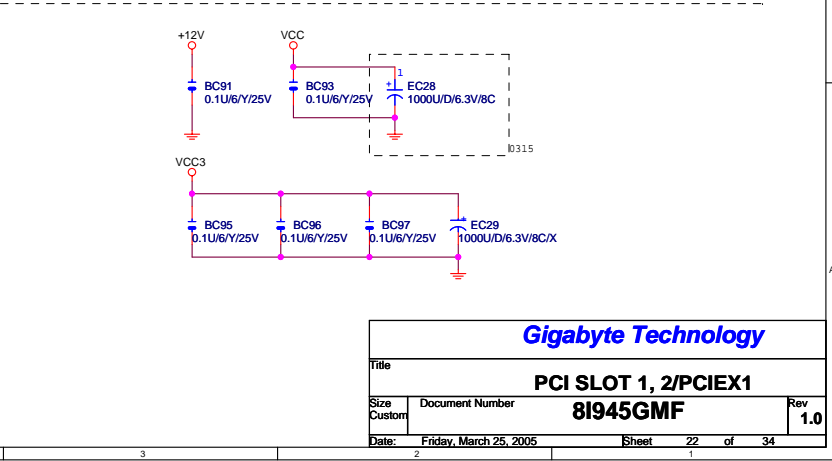
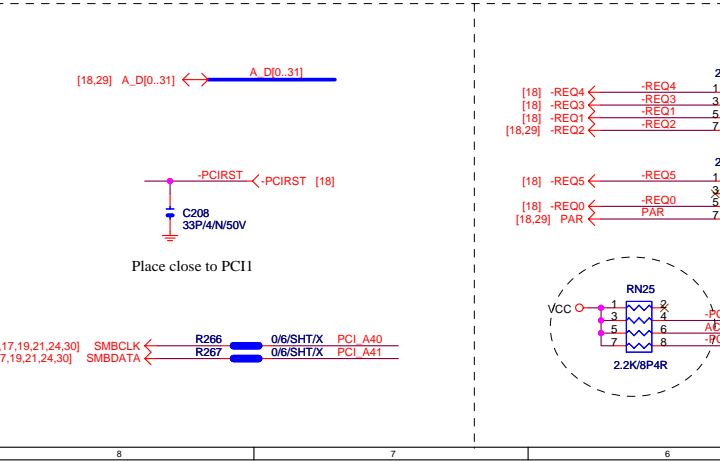
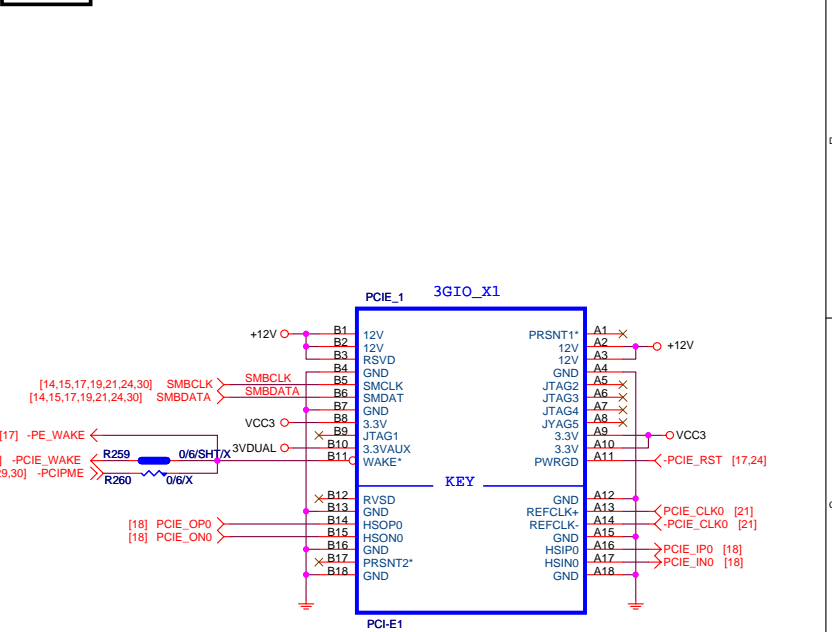
Gigabyte Technology

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PCI1,2 SLOT

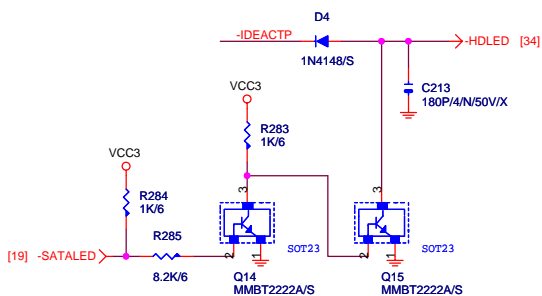


PCIE*1

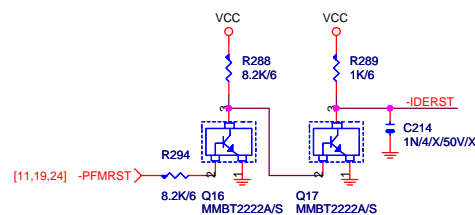


Gigabyte Technology			
Title			
PCI SLOT 1, 2/PCIE*1			
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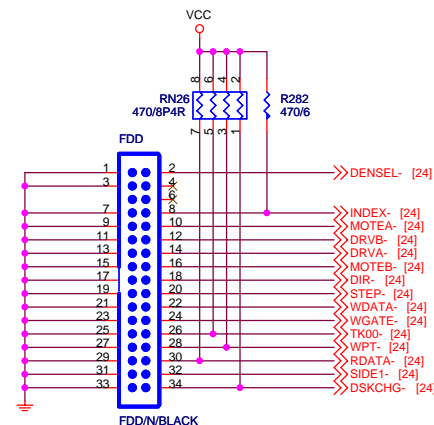
IDE/SATA LED



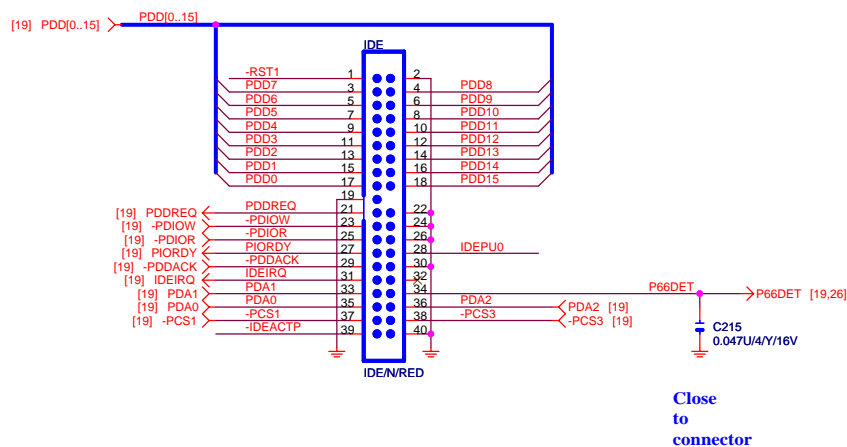
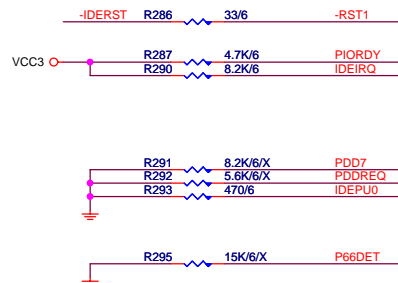
IDE RESET



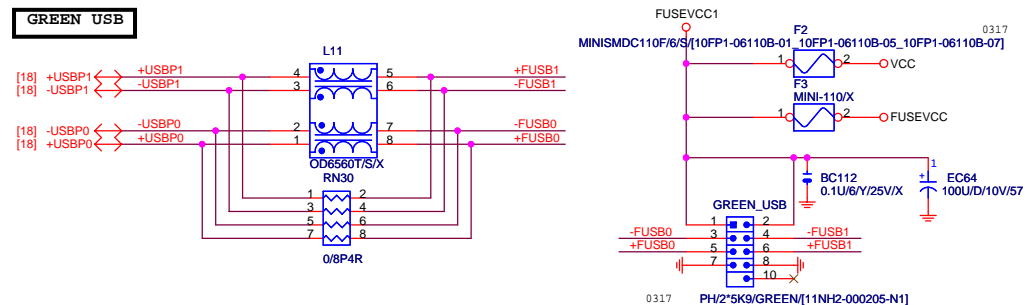
FLOPPY



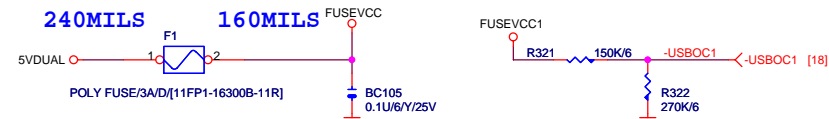
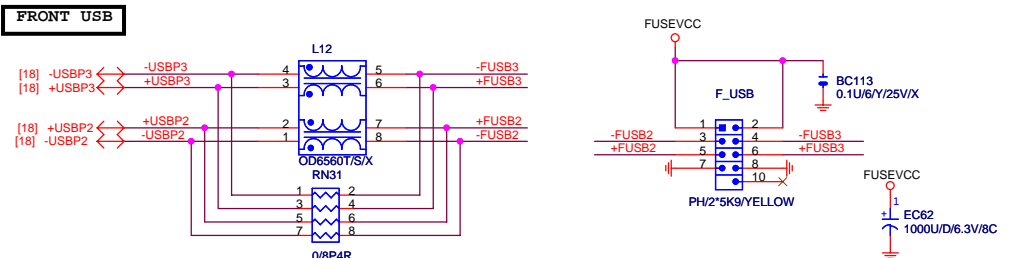
IDE

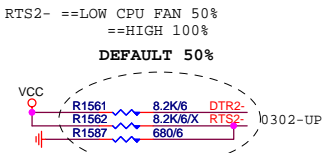


GREEN USB

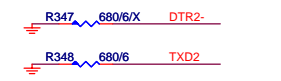


FRONT USB

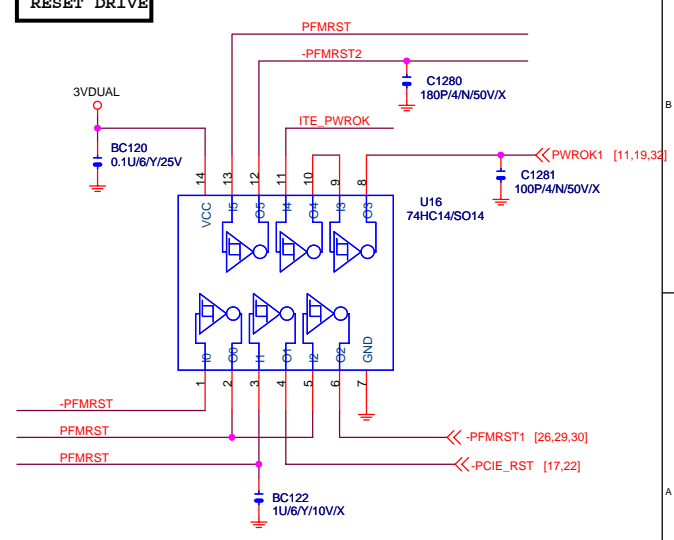
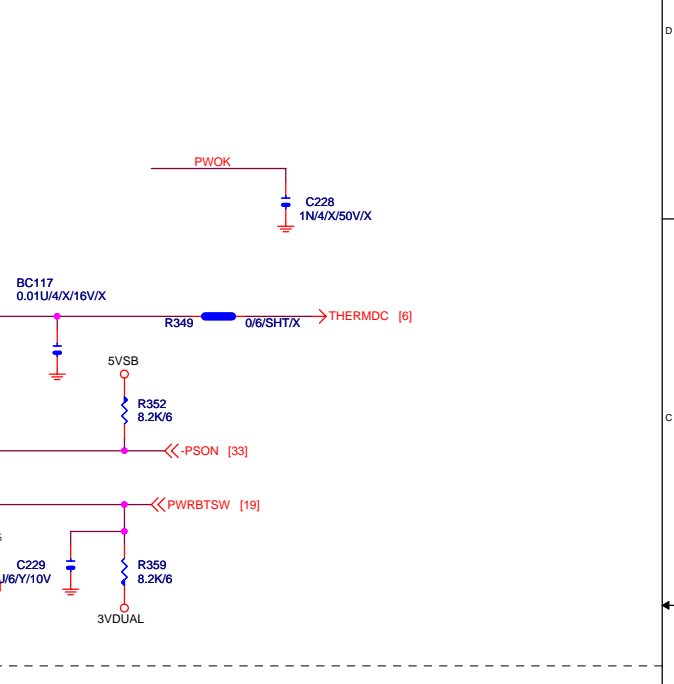
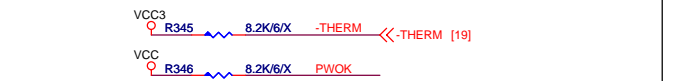
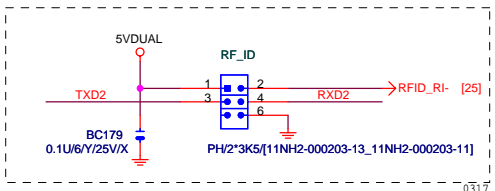
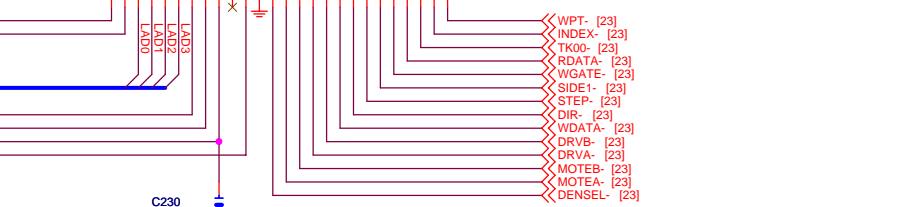
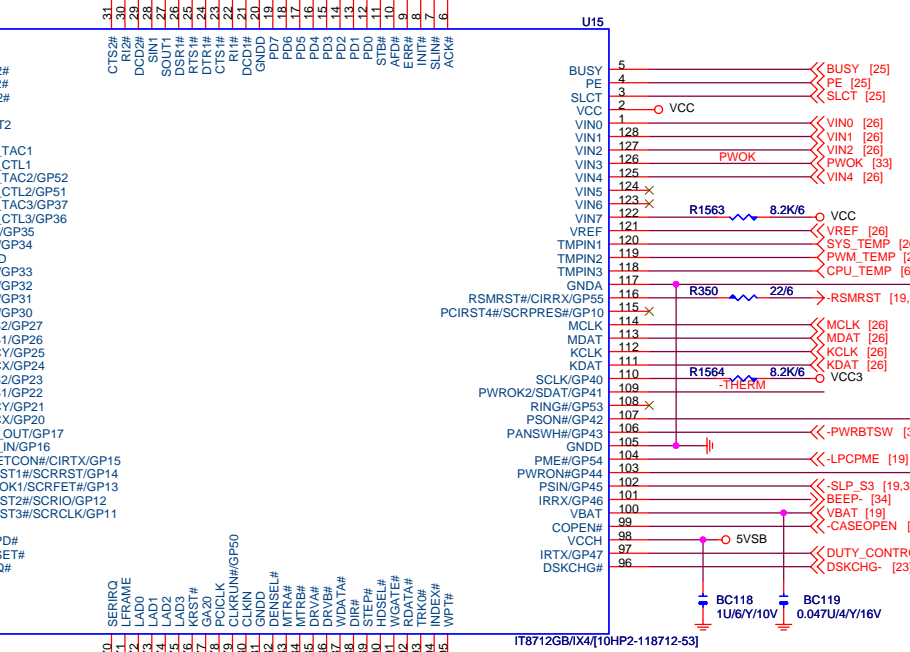
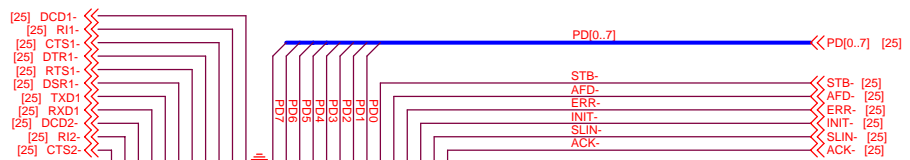
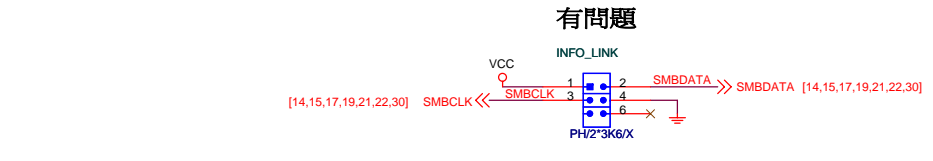
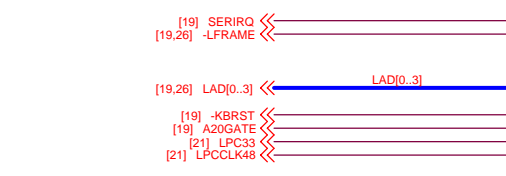
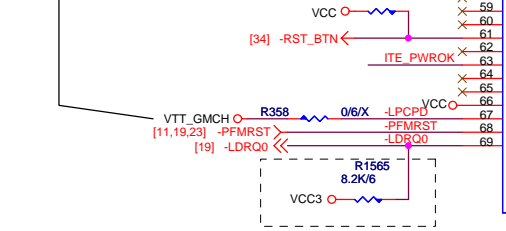




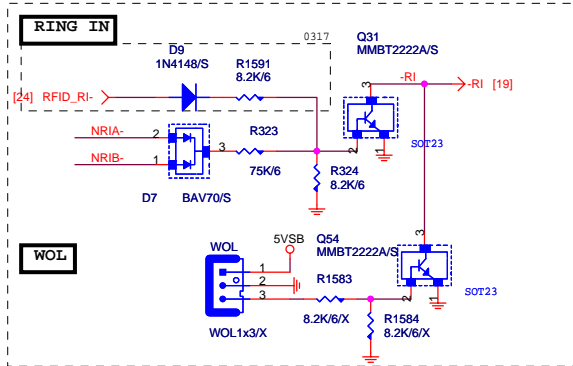
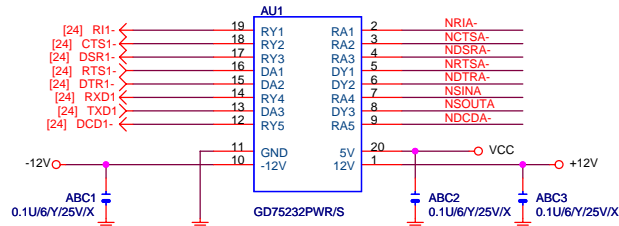
SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.1V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.1V



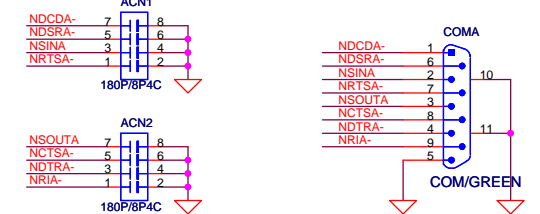
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接 3.3V
LPCPD# = VIDVCC



COMA

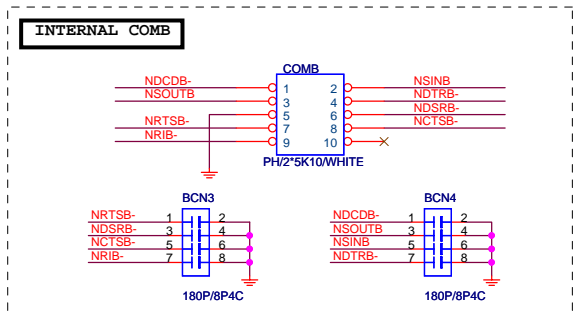
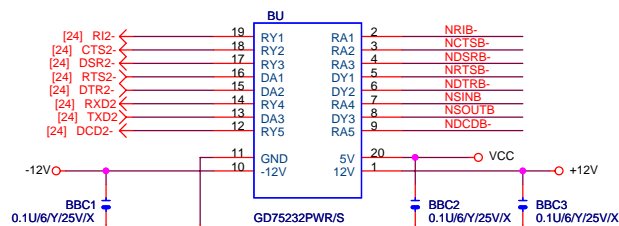


EXTERNAL COMA

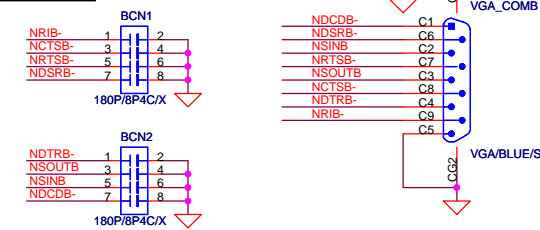


PLACE NEAR COM CONNECTOR

COMB

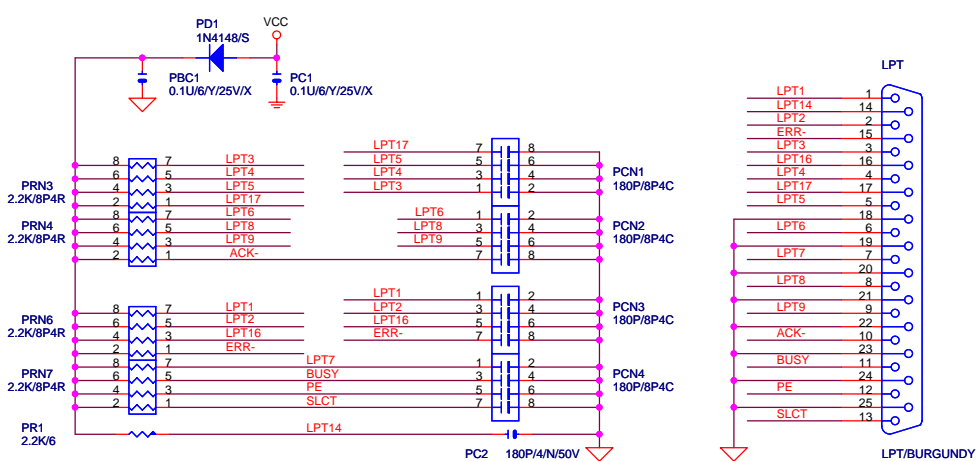
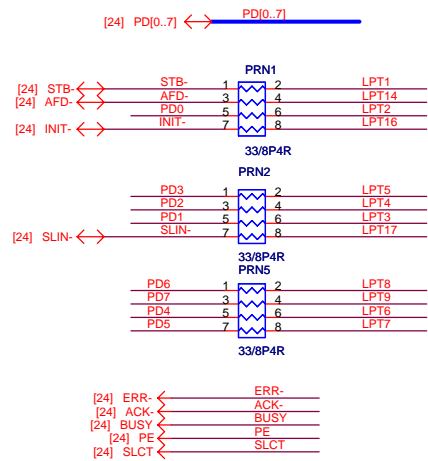


EXTERNAL COMB

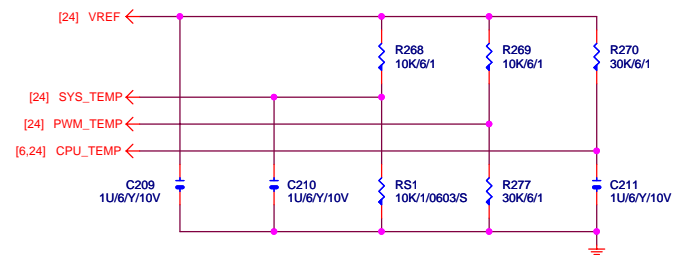


PLACE NEAR VGA_COM CONNECTOR

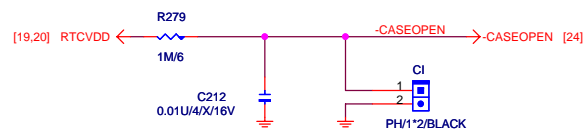
LPT PORT



TEMP H/W MONITOR

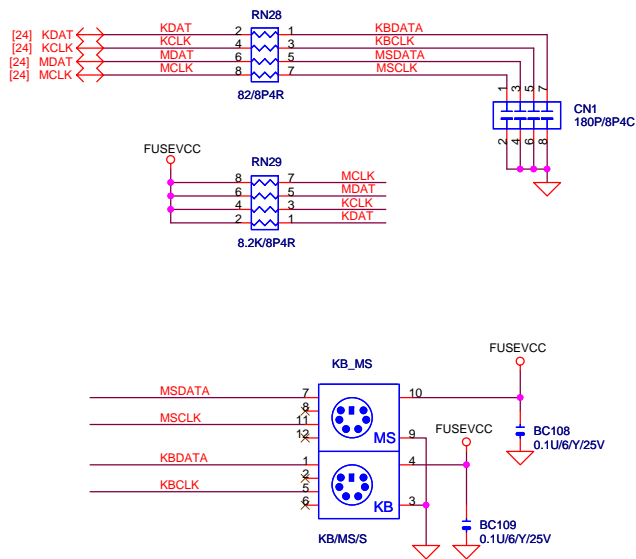


CASE OPEN

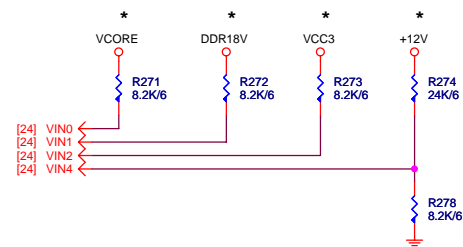


Case Open Circuits

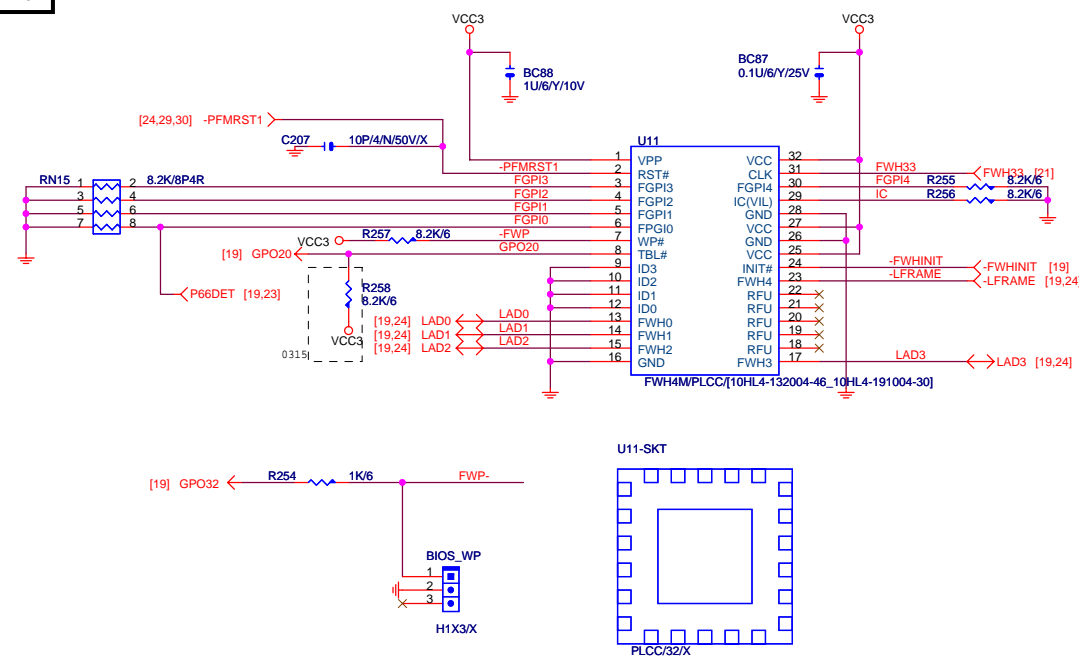
KB/MS

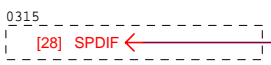


VOLTAGE-- H/W MONITOR

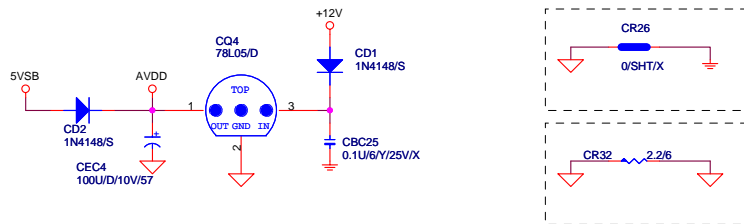


FWM BIOS

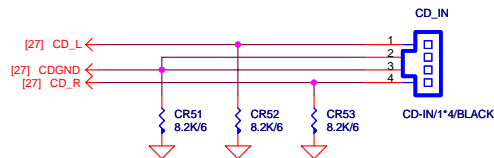




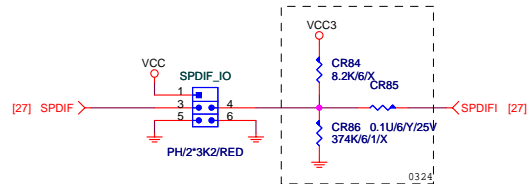
CODEC POWER/EMI PAD



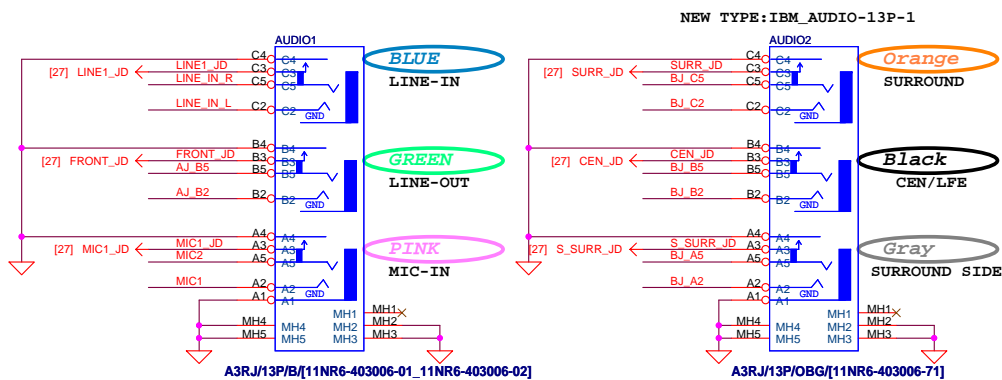
CD IN



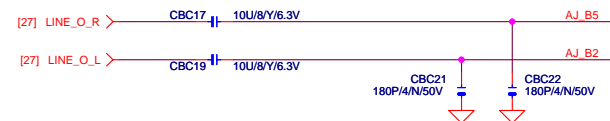
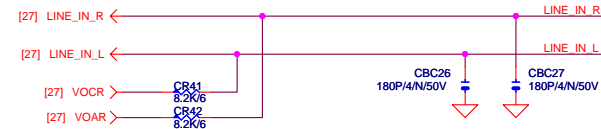
SPDIF



AZALIA JACK



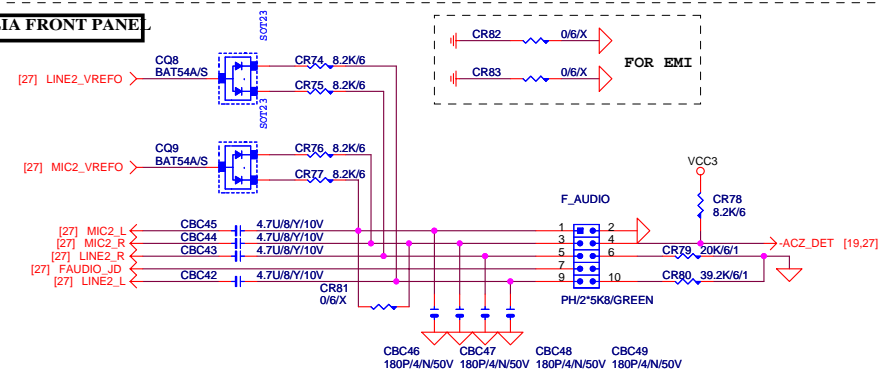
LINE-OUT

**LINE-IN****MIC-IN**

SURROUND

**CEN/LFE**

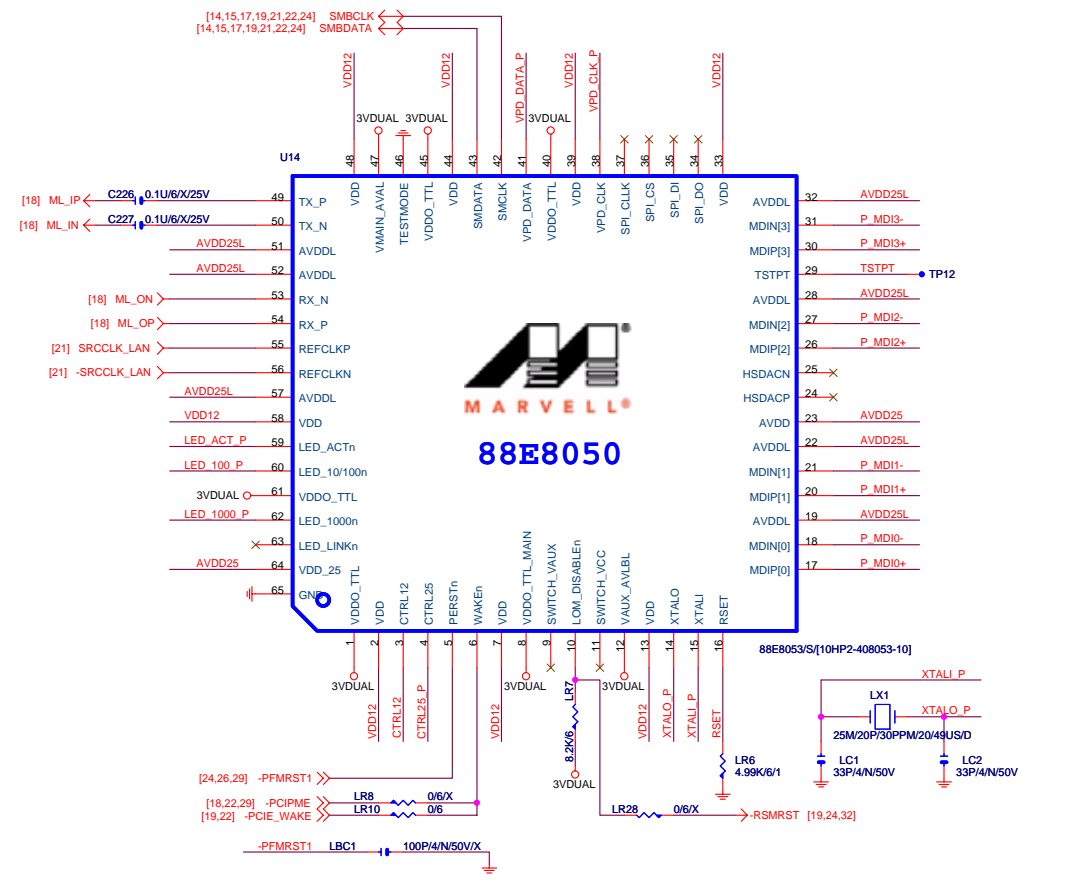
SURR BACK

**AZALIA FRONT PANE**

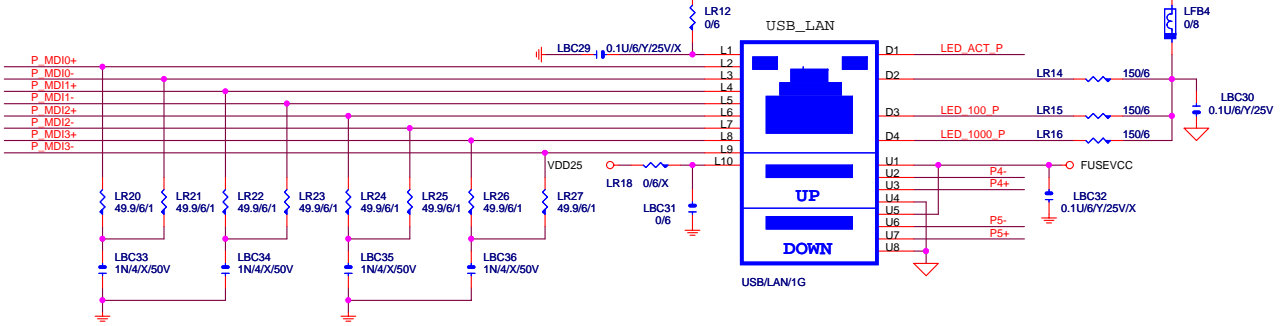
PCIE-1G LAN

Layout Check 注意事項

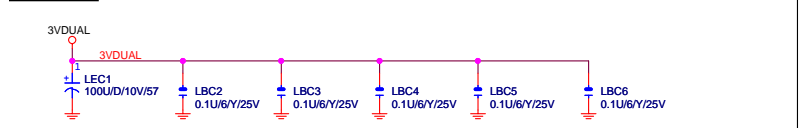
1. LU1 PIN65 需下內層GND, 打 12 VIA
2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
4. MDI正負0~3, TRACE 8:7:8, 每對之間保持 40mil



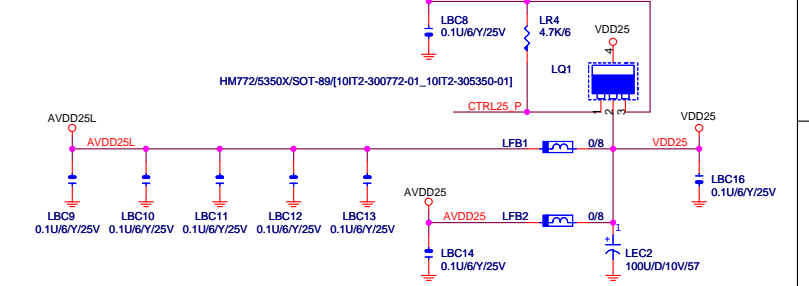
USB_LAN CONNECTOR



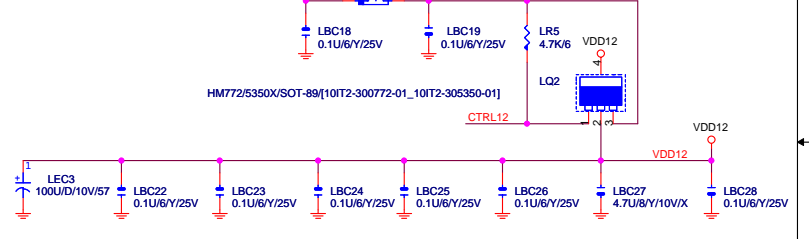
3VDUAL



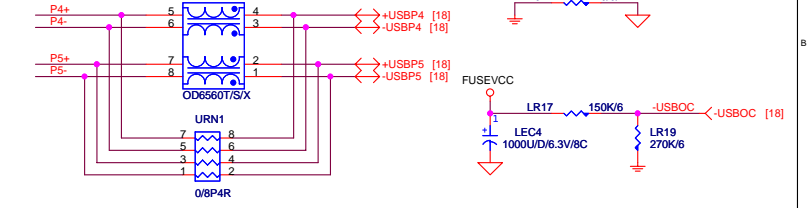
2.5V



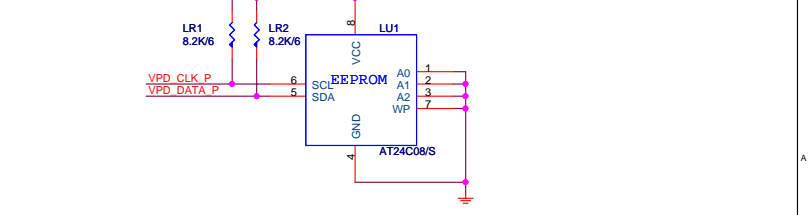
1.2V



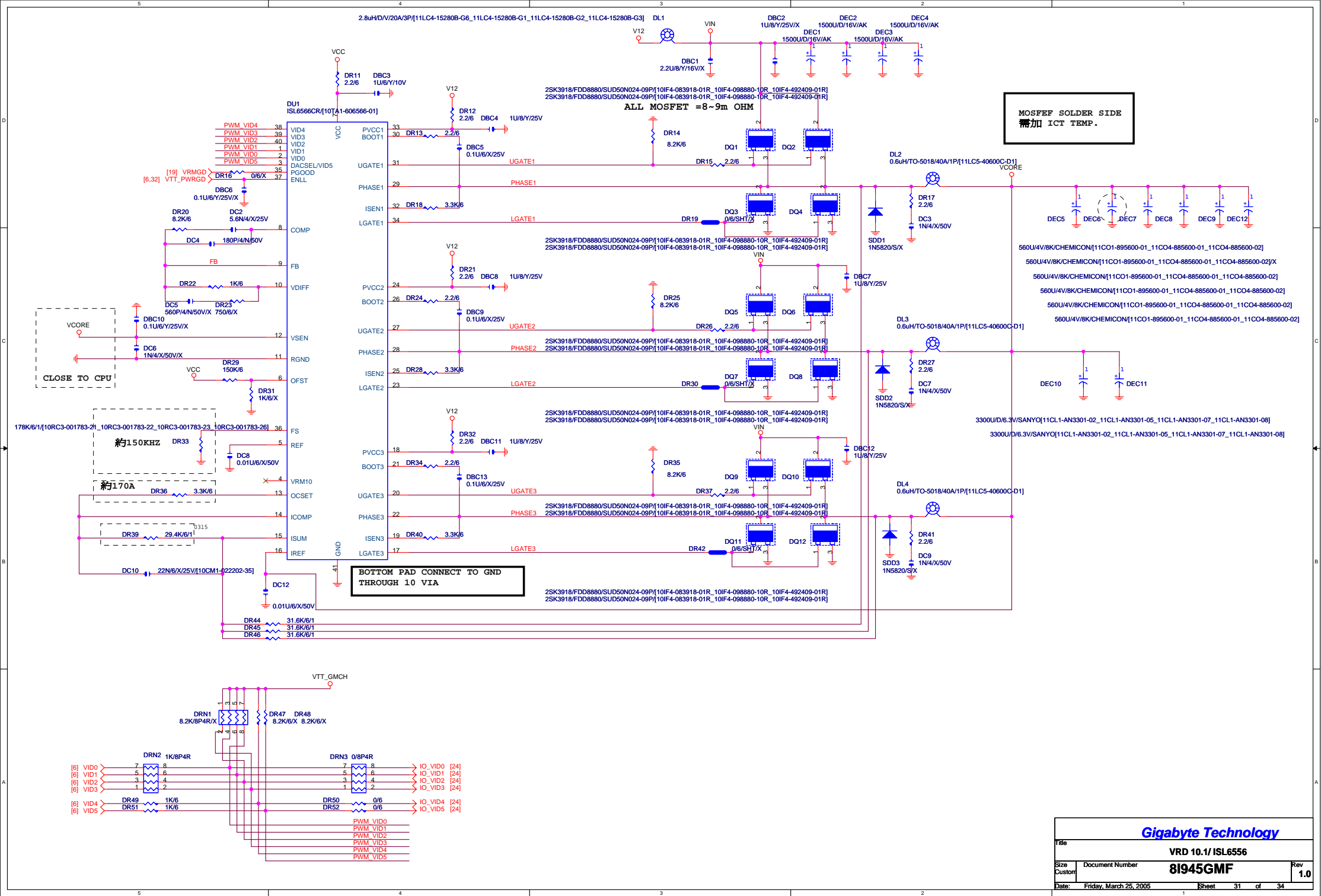
USB_LAN



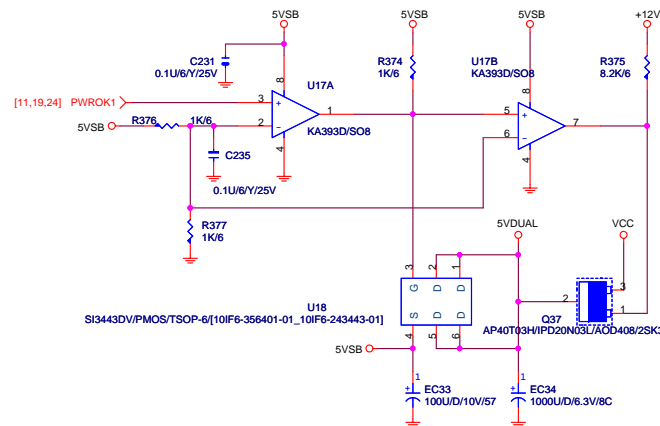
EEPROM



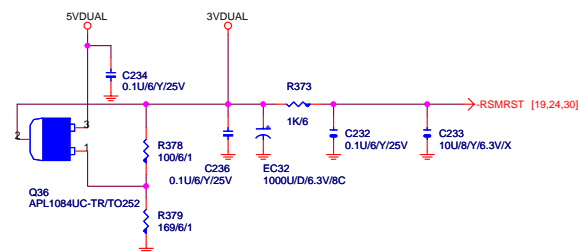
Gigabyte Technology			
Title	MARVELL 88E8001		
Size	Document Number	Rev	
Custom	8I945GMF	1.0	
Date:	Friday, March 25, 2005	Sheet	30 of 34



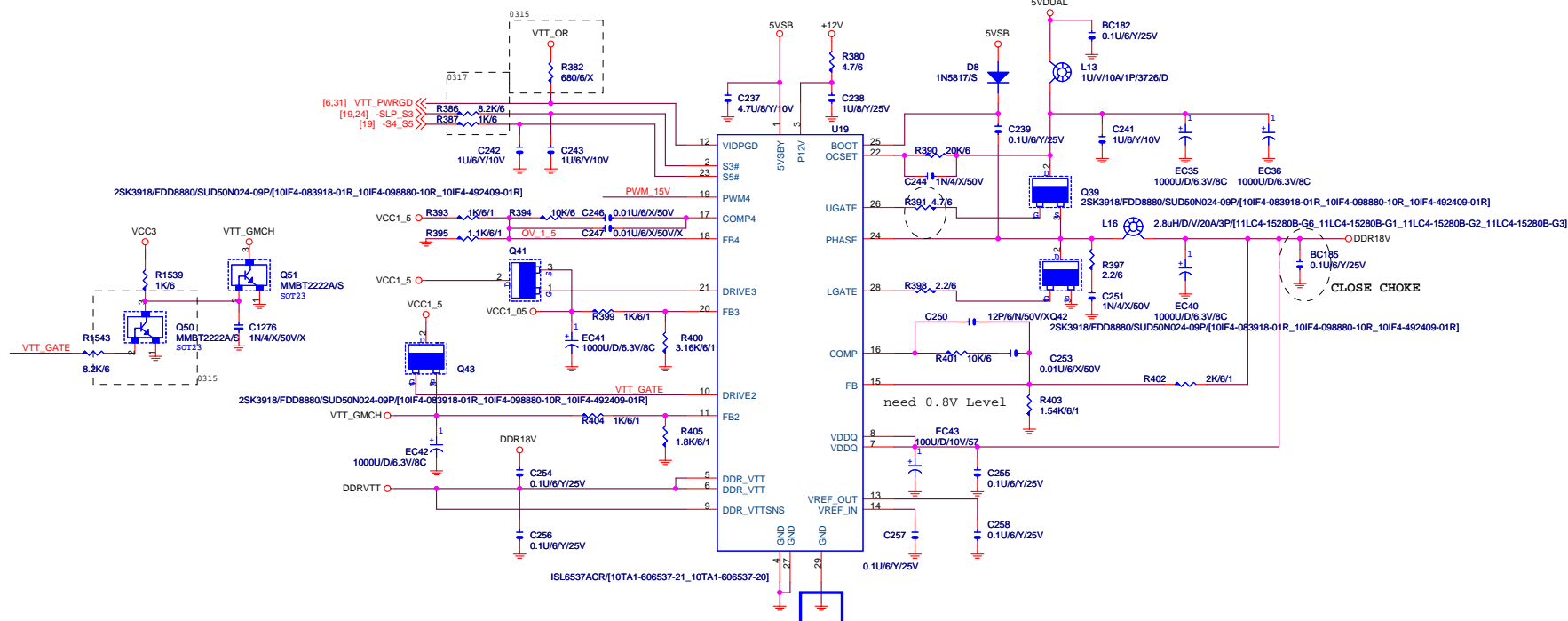
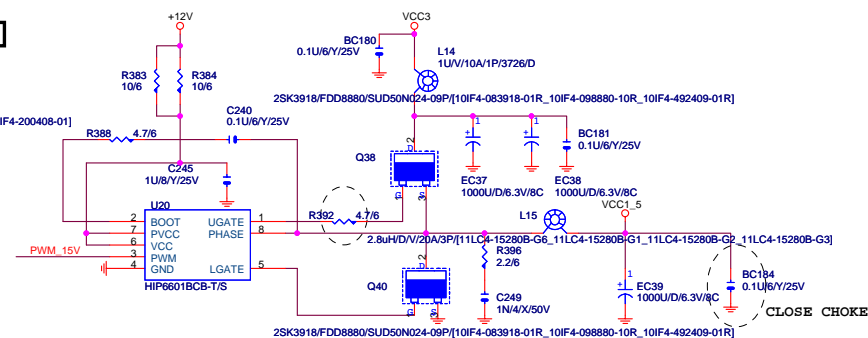
5VDUAL



3VDUAL

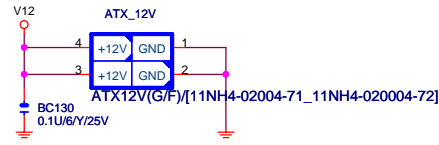
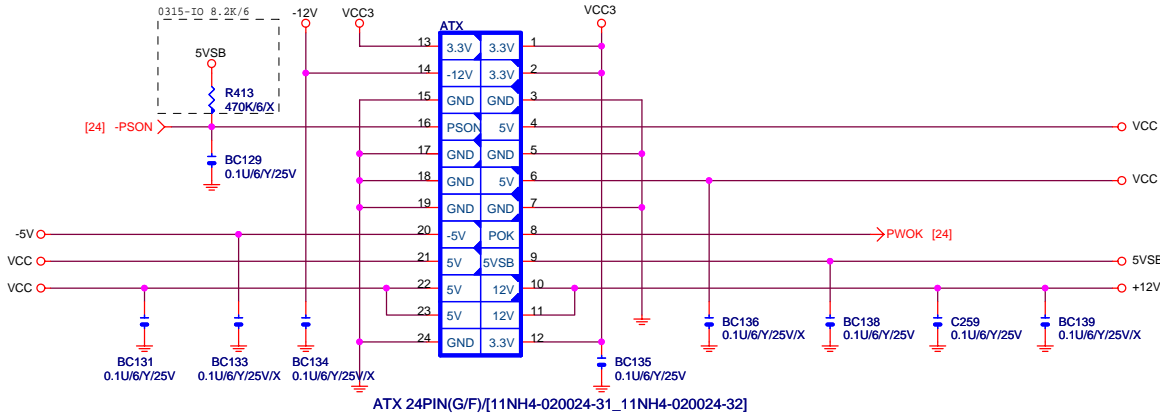


VCC1_5

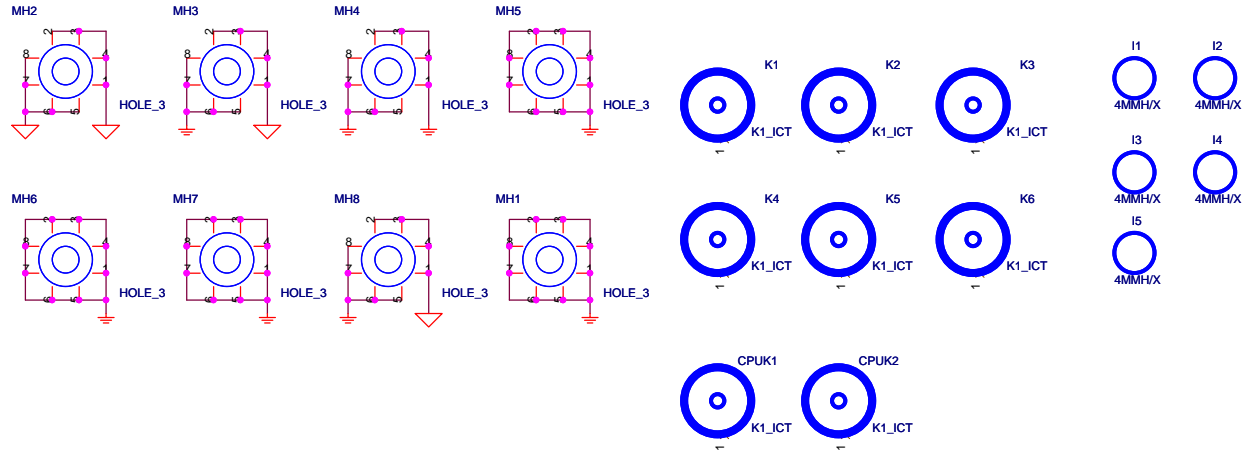


BOTTOM
USE 6 V
CONNECT
GND

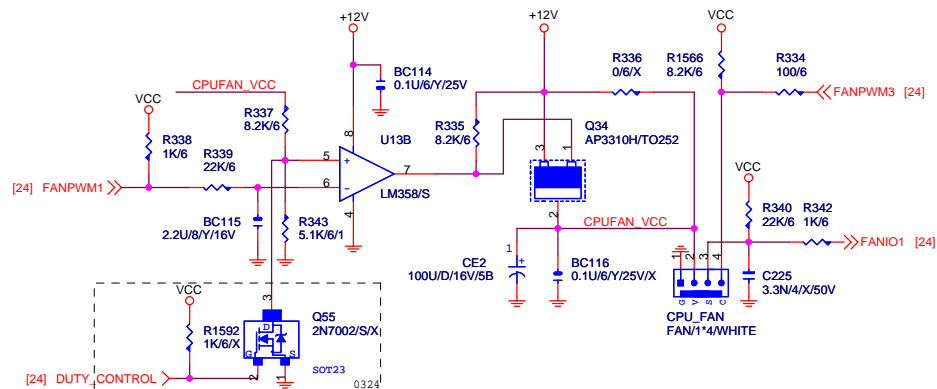
ATX POWER CONNECTOR



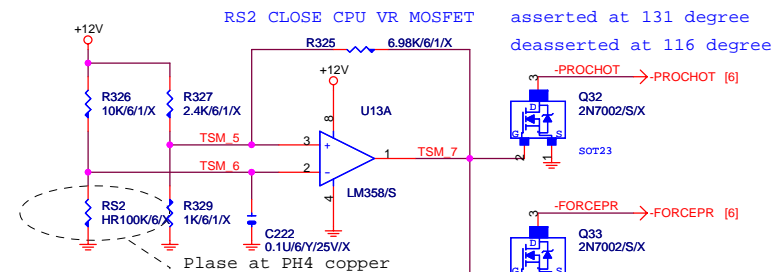
HOLE_3-2--->有鉛



CPU SMART FAN SMART FAN

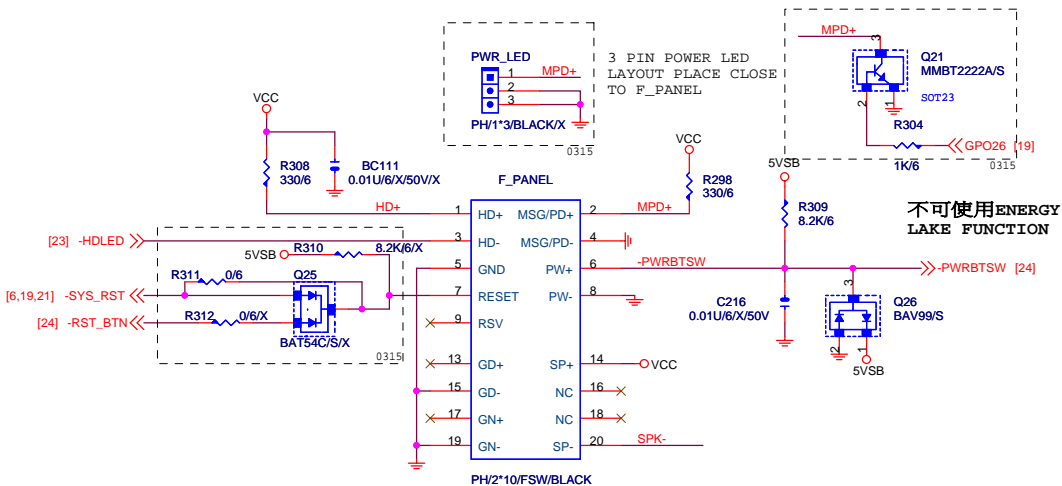


PROCESSOR HOT

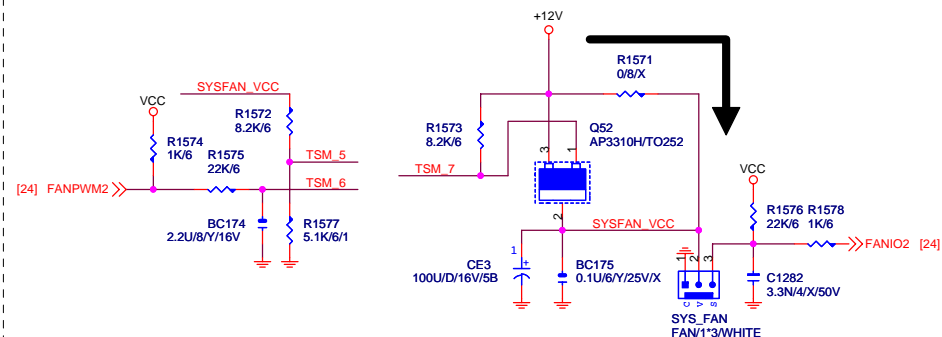


INTEL FRONT PANEL

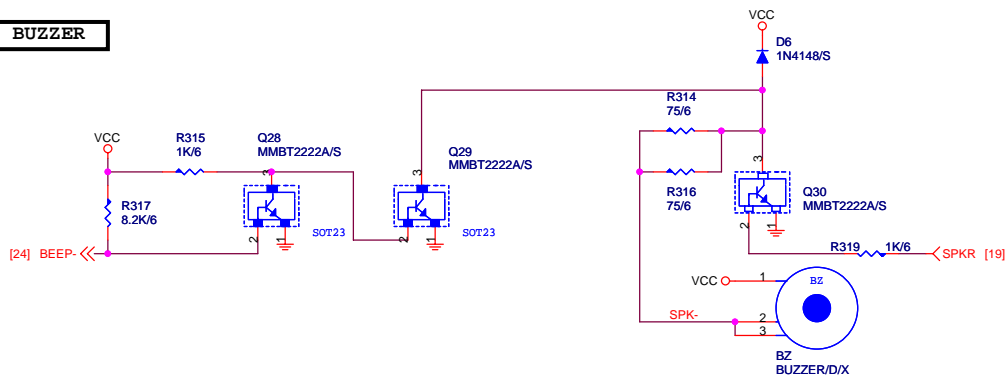
MPD- : (GPIO25--VCCSUS3+HI+HI+DEFINED(C3/C4/S/1/S3/S/4/S5))-->INTEL



SYS_FAN SMART FAN



BUZZER



Gigabyte Technology

Title			FRONT PANEL
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